

## 16M-bit Synchronous DRAM

## Description

The  $\mu$ PD4516421, 4516821, 4516161 are high-speed 16,777,216-bit synchronous dynamic random-access memories, organized as 2,097,152 $\times$ 4 $\times$ 2, 1,048,576 $\times$ 8 $\times$ 2 and 524,288 $\times$ 16 $\times$ 2 (word $\times$ bit $\times$ bank), respectively.

The synchronous DRAMs achieve high-speed data transfer using the pipeline architecture.

All inputs and outputs are synchronized with the positive edge of the clock.

The synchronous DRAMs compatible with Low Voltage TTL (LVTTTL).

The synchronous DRAMs are packaged in 44-pin TSOP (II) ( $\times$ 4,  $\times$ 8) and 50-pin TSOP (II) ( $\times$ 16).

## Features

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Dual internal banks controlled by A11 (Bank Select)
- Programmable burst-length (1, 2, 4, 8 Full Page)
- Programmable wrap sequence (Sequential/Interleave)
- Programmable  $\overline{\text{CAS}}$  latency (1, 2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- $\times$ 4,  $\times$ 8,  $\times$ 16 organization
- Single +3.3 $\pm$ 0.3 V power supply
- LVTTTL compatible
- Byte control ( $\times$ 16) by LDQM and UDQM
- 2,048 refresh cycles/32ms
- Burst termination by Burst Stop command and Precharge command

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**NEC** DATA SHEET *μ*PD4516421, 4516821, 4516161 (PRELIMINARY)

[MEMO]

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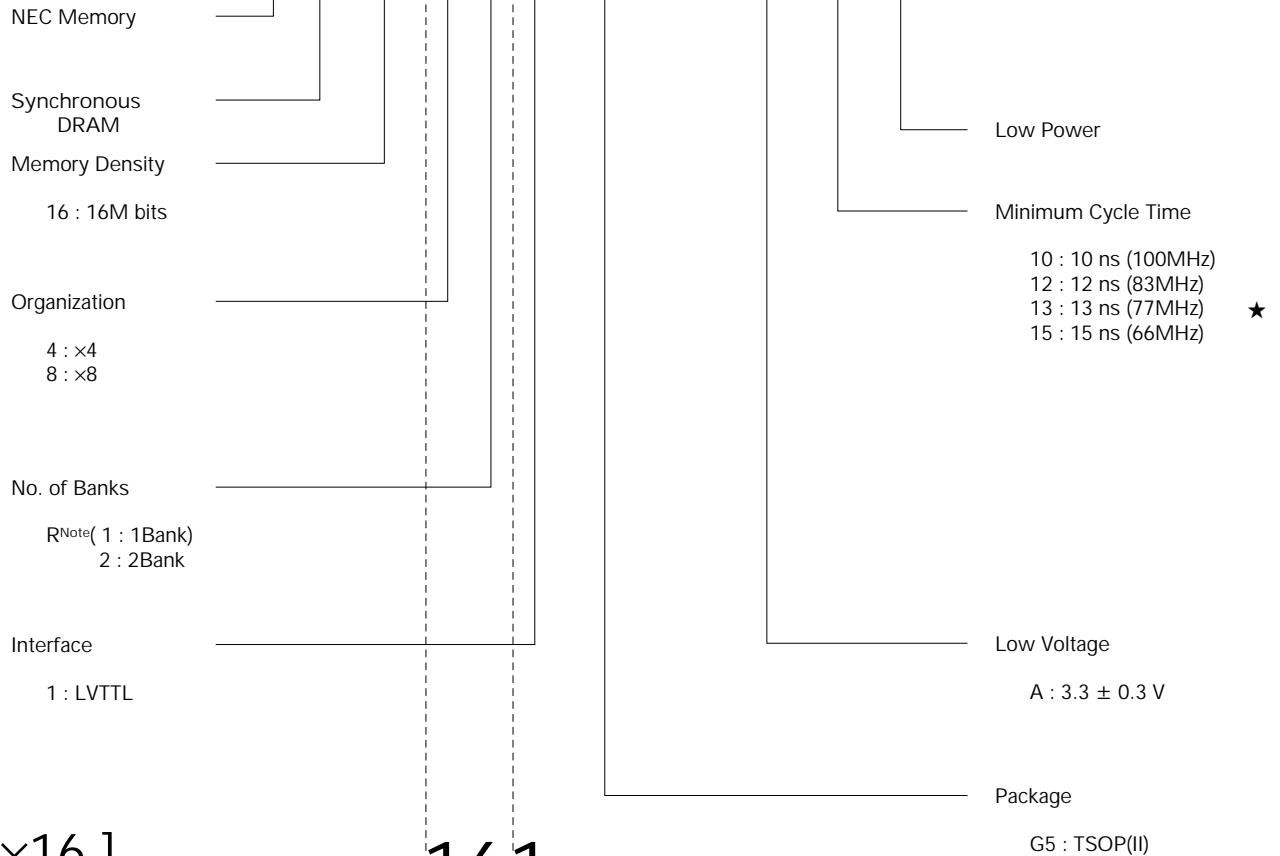
★ Ordering Information

Part number	Organization (word × bit × bank)	Clock frequency MHz (MAX.)	Package
μPD4516421G5-A10-7JF	2M×4×2	100	44-pin Plastic TSOP(II) (400mil)
μPD4516421G5-A12-7JF		83	
μPD4516421G5-A13-7JF		77	
μPD4516421G5-A15-7JF		66	
μPD4516821G5-A10-7JF	1M×8×2	100	44-pin Plastic TSOP(II) (400mil)
μPD4516821G5-A12-7JF		83	
μPD4516821G5-A13-7JF		77	
μPD4516821G5-A15-7JF		66	
μPD4516161G5-A10-7JF	512K×16×2	100	50-pin Plastic TSOP(II) (400mil)
μPD4516161G5-A12-7JF		83	
μPD4516161G5-A13-7JF		77	
μPD4516161G5-A15-7JF		66	

Part Number

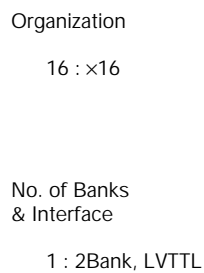
[ ×4, ×8 ]

# μPD4516821G5 - A10L



[ ×16 ]

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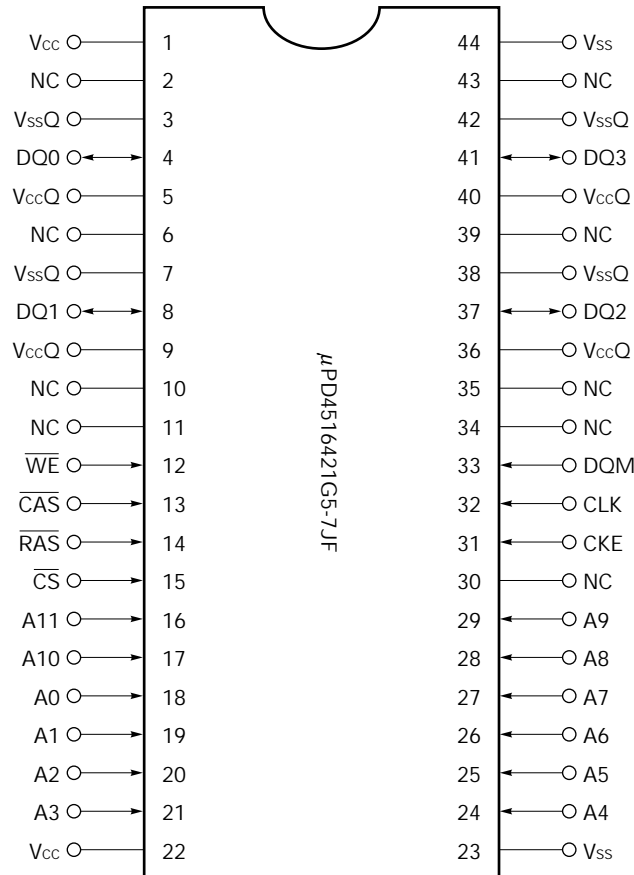


Note R: Reserved

★ Pin Configurations

[μPD4516421]

44-pin Plastic TSOP(II) (400 mil)

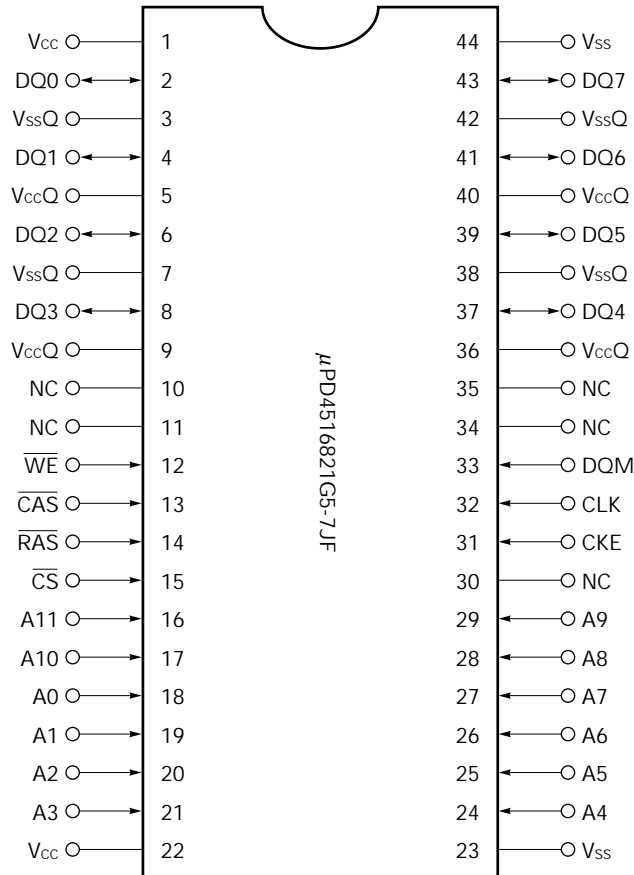


- A0 to A11<sup>Note</sup> : Address inputs
- DQ0 to DQ3 : Data inputs/outputs
- CLK : System clock input
- CKE : Clock enable
- $\overline{CS}$  : Chip select
- $\overline{RAS}$  : Row address strobe
- $\overline{CAS}$  : Column address strobe
- $\overline{WE}$  : Write enable
- DQM : DQ mask enable
- Vcc : Supply voltage
- Vss : Ground
- VccQ : Supply voltage for DQ
- VssQ : Ground for DQ
- NC : No connection

- Note A0 to A10: Row address inputs
- A0 to A9 : Column address inputs
- A11 : Bank select

[μPD4516821]

44-pin Plastic TSOP(II) (400 mil)

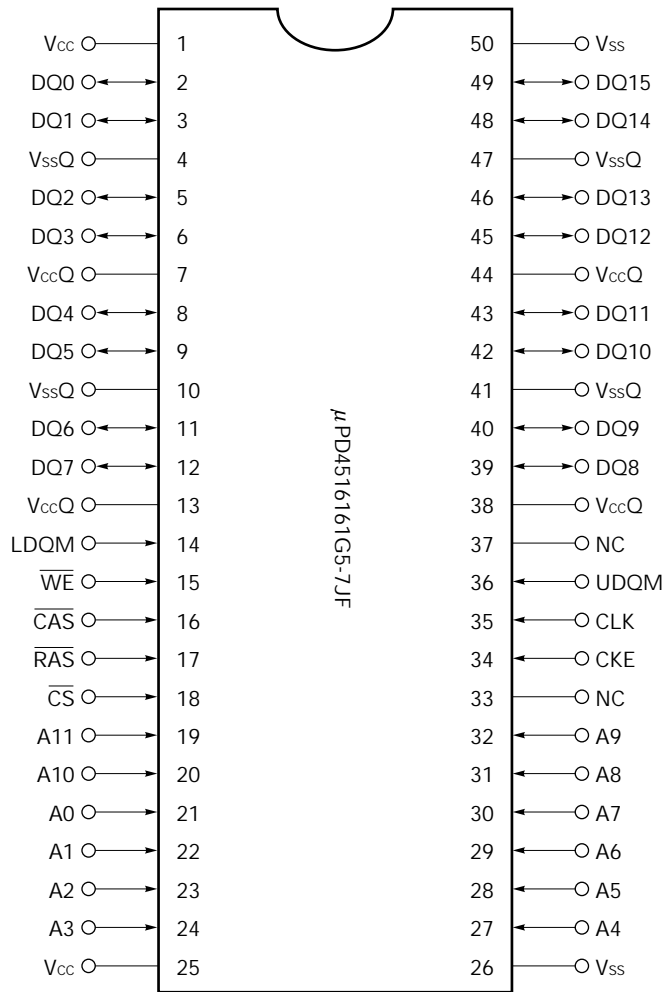


- A0 to A11 : Address inputs
- DQ0 to DQ7 : Data inputs/outputs
- CLK : System clock input
- CKE : Clock enable
- CS : Chip select
- RAS : Row address strobe
- CAS : Column address strobe
- WE : Write enable
- DQM : DQ mask enable
- Vcc : Supply voltage
- Vss : Ground
- VccQ : Supply voltage for DQ
- VssQ : Ground for DQ
- NC : No connection

Note A0 to A10: Row address inputs  
 A0 to A8 : Column address inputs  
 A11 : Bank select

[μPD4516161]

50-pin Plastic TSOP(II) (400 mil)



- A0 to A11 : Address inputs
- DQ0 to DQ15 : Data inputs/outputs
- CLK : System clock input
- CKE : Clock enable
- $\overline{CS}$  : Chip select
- $\overline{RAS}$  : Row address strobe
- $\overline{CAS}$  : Column address strobe
- $\overline{WE}$  : Write enable
- UDQM : Upper DQ mask enable
- LDQM : Lower DQ mask enable
- Vcc : Supply voltage
- Vss : Ground
- VccQ : Supply voltage for DQ
- VssQ : Ground for DQ
- NC : No connection

- Note
- A0 to A10 : Row address inputs
  - A0 to A7 : Column address inputs
  - A11 : Bank select



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1. Input/Output Pin Function

Pin name	Input/Output	Function
CLK	Input	CLK is the master clock input. Other inputs signals are referenced to the CLK rising edge.
CKE	Input	CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not asserted and the μPD4516xxx suspends operation. When the μPD4516xxx is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low.
$\overline{CS}$	Input	$\overline{CS}$ low starts the command input cycle. When $\overline{CS}$ is high, commands are ignored but operations continue.
$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	Input	$\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ have the same symbols on conventional DRAM but different functions. For details, refer to the command table.
A0 - A11	Input	Row Address is determined by A0 - A10 at the CLK (clock) rising edge in the activate command cycle. It does not depend on the bit organization. Column Address is determined by A0 - A9 at the CLK rising edge in the read or write command cycle. It depends on the bit organization: A0 - A9 for ×4 device, A0 - A8 for ×8 device and A0 - A7 for ×16 device. A11 is the bank select signal (BS). In command cycle, A11 low selects bank A and A11 high selects bank B. A10 defines the precharge mode. When A10 is high in the precharge command cycle, both banks are precharged; when A10 is low, only the bank selected by A11 is precharged. When A10 high in read or write command cycle, the precharge start automatically after the burst access.
DQM UDQM LDQM	Input	DQM controls I/O buffers. In ×16 products, UDQM and LDQM control upper byte and lower byte I/O buffers, respectively. In read mode, DQM controls the output buffers like a conventional $\overline{OE}$ pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the read is two clocks. In write mode, DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.
DQ0 - DQ15	Input/Output	DQ pins have the same function as I/O pins on a conventional DRAM.
V <sub>cc</sub> V <sub>ss</sub> V <sub>ccQ</sub> V <sub>ssQ</sub>	(Power supply)	V <sub>cc</sub> and V <sub>ss</sub> are power supply pins for internal circuits. V <sub>ccQ</sub> and V <sub>ssQ</sub> are power supply pins for the output buffers.

2. Commands

Mode register set command

$$(\overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE} = \text{Low})$$

The μPD4516xxx has a mode register that defines how the device operates. In this command, A0 through A11 are the data input pins. After power on, the mode register set command must be executed to initialize the device.

The mode register can be set only when both banks are in idle state.

During the two cycles following this command, the μPD4516xxx cannot accept any other commands.

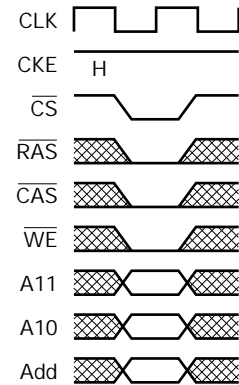


Fig. 1 Mode register set command

Activate command

$$(\overline{CS}, \overline{RAS} = \text{Low}, \overline{CAS}, \overline{WE} = \text{High})$$

The μPD4516xxx has two banks, each with 2048 rows.

This command activates the bank selected by A11 (BS) and a row address selected by A0 through A10.

This command corresponds to a conventional DRAM's  $\overline{RAS}$  falling.

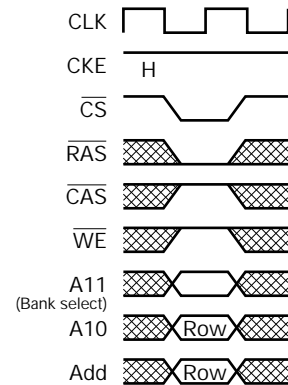


Fig. 2 Row address strobe and bank active command

Precharge command

$$(\overline{CS}, \overline{RAS}, \overline{WE} = \text{Low}, \overline{CAS} = \text{High})$$

This command begins precharge operation of the bank selected by A11 (BS) and A10. When A10 is High, both banks are precharged, regardless of A11. When A10 is Low, only the bank selected by A11 is precharged. A11 low selects bank A and A11 high selects bank B.

After this command, the μPD4516xxx can't accept the activate command to the precharging bank during  $t_{RP}$  (precharge to activate command period).

This command corresponds to a conventional DRAM's RAS rising.

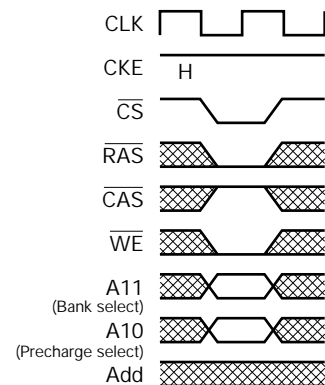


Fig. 3 Precharge command

Write command

$$(\overline{CS}, \overline{CAS}, \overline{WE} = \text{Low}, \overline{RAS} = \text{High})$$

If the mode register is in the burst write mode, this command sets the burst start address given by the column address to begin the burst write operation. The first write data must be input with this write operation. The first write data in burst mode can input with this command with subsequent data on following clocks.

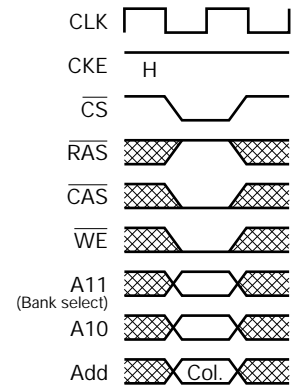


Fig. 4 Column address and write command

Read command

$$(\overline{CS}, \overline{CAS} = \text{Low}, \overline{RAS}, \overline{WE} = \text{High})$$

This command sets the burst start address given by the column address.

Read data is available after  $\overline{CAS}$  latency requirements have been met.

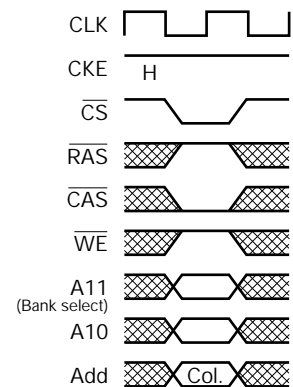


Fig. 5 Column address and read command

CBR (auto) refresh command

$$(\overline{CS}, \overline{RAS}, \overline{CAS} = \text{Low}, \overline{WE}, \text{CKE} = \text{High})$$

This command is a request to begin the CBR refresh operation. The refresh address and the bank select address are generated internally.

Before executing CBR refresh, both banks must be precharged.

After this cycle, both banks will be in the idle (precharged) state and ready for a row activate command.

During  $t_{RC}$  period (from refresh command to refresh or activate command), the μPD4516xxx cannot accept any other command.

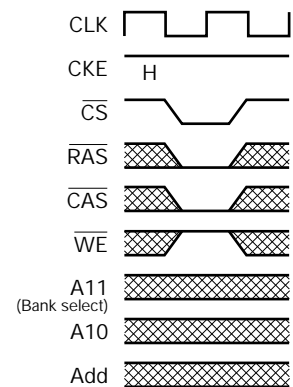


Fig. 6 Auto refresh command

Self refresh entry command

$$(\overline{CS}, \overline{RAS}, \overline{CAS}, \text{CKE} = \text{Low}, \overline{WE} = \text{High})$$

After the command execution, self refresh operation continues while CKE remains low. When CKE goes high, the μPD4516xxx exits the self refresh mode.

During self refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control.

Before executing self refresh, both banks must be precharged.

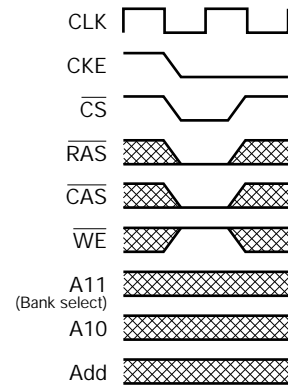


Fig. 7 Self refresh entry command

Burst stop command

$$(\overline{CS}, \overline{WE} = \text{Low}, \overline{RAS}, \overline{CAS} = \text{High})$$

This command terminates the current burst operation.

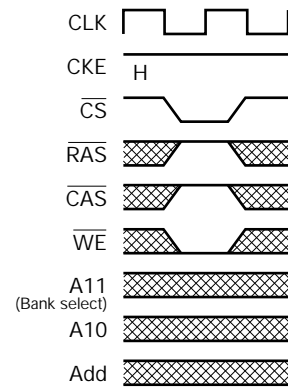


Fig. 8 Burst stop command in Full Page mode

No operation

$$(\overline{CS} = \text{Low}, \overline{RAS}, \overline{CAS}, \overline{WE} = \text{High})$$

This command is not an execution command. No operations begin or terminate by this command.

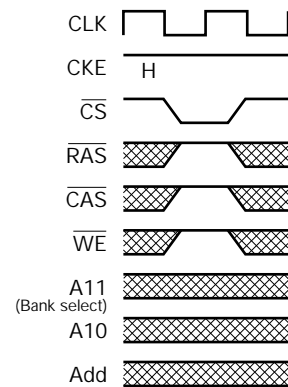
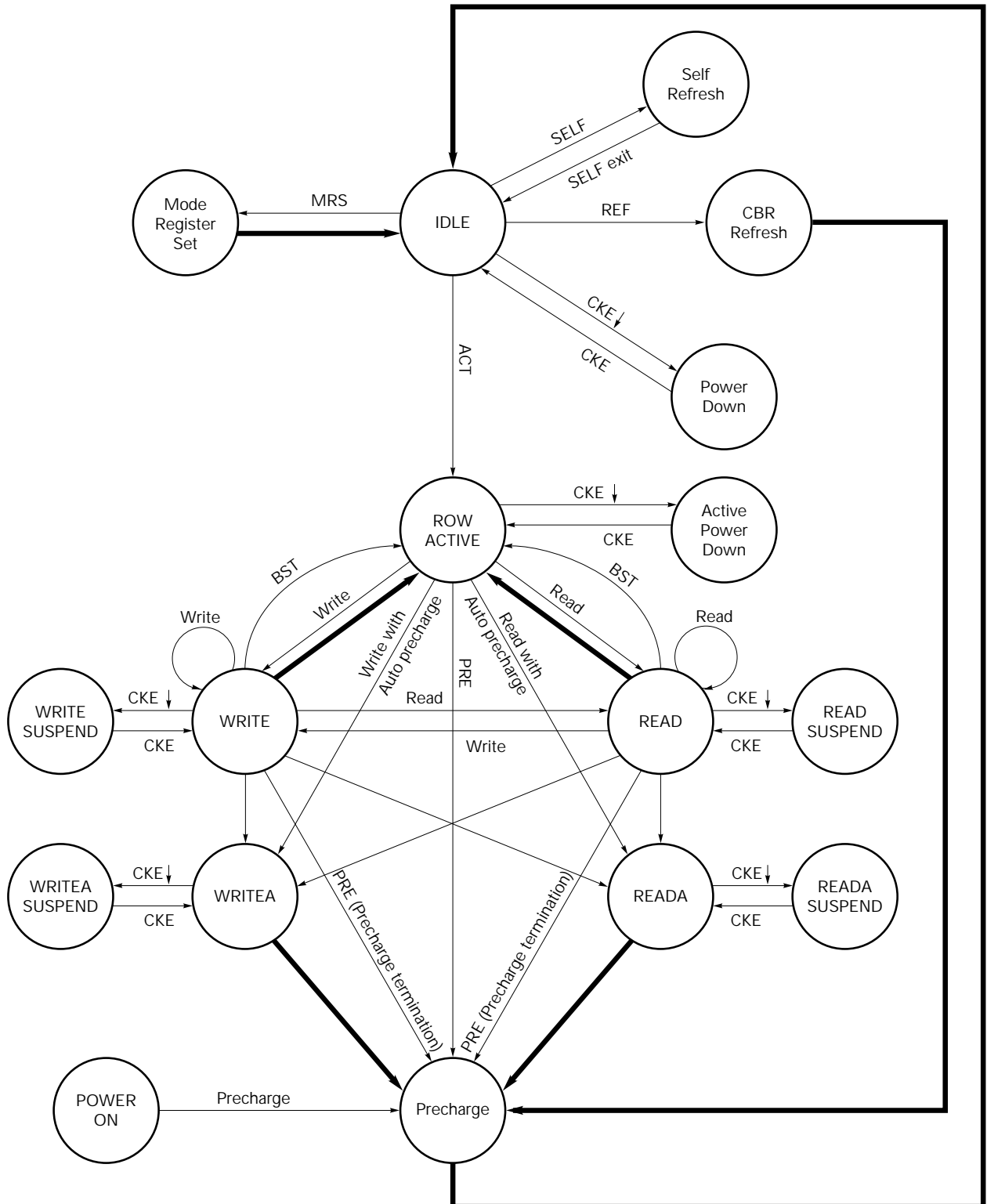




Fig. 9 No operation

3. Simplified State Diagram



 Automatic sequence  
 Manual input

4. Truth Table

4.1 Command Truth Table

Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A9-A0
		n-1	n							
Device deselect	DESL	H	x	H	x	x	x	x	x	x
No operation	NOP	H	x	L	H	H	H	x	x	x
Burst stop	BST	H	x	L	H	H	L	x	x	x
Read	READ	H	x	L	H	L	H	V	L	V
Read with auto precharge	READA	H	x	L	H	L	H	V	H	V
Write	WRIT	H	x	L	H	L	L	V	L	V
Write with auto precharge	WRITA	H	x	L	H	L	L	V	H	V
Bank activate	ACT	H	x	L	L	H	H	V	V	V
Precharge select bank	PRE	H	x	L	L	H	L	V	L	x
Precharge all banks	PALL	H	x	L	L	H	L	x	H	x
Mode register set	MRS	H	x	L	L	L	L	L	L	V

4.2 DQM Truth Table

Function	Symbol	CKE		DQM	
		n-1	n	U	L
Data write/output enable	ENB	H	x	L	
Data mask/output disable	MASK	H	x	H	
Upper byte write enable/output enable	ENBU	H	x	L	x
Lower byte write enable/output enable	ENBL	H	x	x	L
Upper byte write inhibit/output disable	MASKU	H	x	H	x
Lower byte write inhibit/output disable	MASKL	H	x	x	H

4.3 CKE Truth Table

Current state	Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
			n-1	n					
Activating	Clock suspend mode entry		H	L	x	x	x	x	x
Any	Clock suspend		L	L	x	x	x	x	x
Clock suspend	Clock suspend mode exit		L	H	x	x	x	x	x
Idle	CBR refresh command	REF	H	H	L	L	L	H	x
Idle	Self refresh entry	SELF	H	L	L	L	L	H	x
Self refresh	Self refresh exit		L	H	L	H	H	H	x
			L	H	H	x	x	x	x
Idle	Power down entry		H	L	x	x	x	x	x
Power down	Power down exit		L	H	x	x	x	x	x

H: High level, L: Low level

x: High or Low level (Don't care), V: Valid Data input



4.4 Operative Command Table<sup>Notes1, 2</sup>

(1/3)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Idle	H	x	x	x	x	DESL	Nop or Power down	3
	L	H	H	x	x	NOP or BST	Nop or Power down	3
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	4
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	H	H	BA, RA	ACT	Row active	
	L	L	H	L	BA, A10	PRE/PALL	Nop	
	L	L	L	H	x	REF/SELF	Refresh or Self refresh	5
	L	L	L	L	Op-Code	MRS	Mode register access	
Row active	H	x	x	x	x	DESL	Nop	
	L	H	H	x	x	NOP or BST	Nop	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read:Determine AP	6
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Begin write:Determine AP	6
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	Precharge	7
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Read	H	x	x	x	x	DESL	Continue burst to end → Row active	
	L	H	H	H	x	NOP	Continue burst to end → Row active	
	L	H	H	L	x	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Term burst, new read:Determine AP	8
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Term burst, start write:Determine AP	8, 9
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	Term burst, precharging	
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write	H	x	x	x	x	DESL	Continue burst to end → Write recovering	
	L	H	H	H	x	NOP	Continue burst to end → Write recovering	
	L	H	H	L	x	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Term burst, start read:Determine AP	8, 9
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Term burst, new write:Determine AP	8
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	Term burst precharging	10
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Read with auto precharge	H	x	x	x	x	DESL	Continue burst to end → Precharging	
	L	H	H	H	x	NOP	Continue burst to end → Precharging	
	L	H	H	L	x	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write with auto precharge	H	x	x	x	x	DESL	Continue burst to end → Write recovering with auto precharge	
	L	H	H	H	x	NOP	Continue burst to end → Write recovering with auto precharge	
	L	H	H	L	x	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Precharging	H	x	x	x	x	DESL	Nop → Enter idle after $t_{RP}$	
	L	H	H	H	x	NOP	Nop → Enter idle after $t_{RP}$	
	L	H	H	L	x	BST	Nop → Enter idle after $t_{RP}$	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	4
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after $t_{RP}$	
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Row activating	H	x	x	x	x	DESL	Nop → Enter row active after $t_{RCD}$	
	L	H	H	H	x	NOP	Nop → Enter row active after $t_{RCD}$	
	L	H	H	L	x	BST	Nop → Enter row active after $t_{RCD}$	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	4
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	H	H	BA, RA	ACT	ILLEGAL	4, 11
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Write recovering	H	x	x	x	x	DESL	Nop → Enter row active after t <sub>DPL</sub>	
	L	H	H	H	x	NOP	Nop → Enter row active after t <sub>DPL</sub>	
	L	H	H	L	x	BST	Nop → Enter row active after t <sub>DPL</sub>	
	L	H	L	H	BA, CA, A10	READ/READA	Start read, Determine AP	9
	L	H	L	L	BA, CA, A10	WRIT/WRITA	New write, Determine AP	
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write recovering with auto precharge	H	x	x	x	x	DESL	Nop → Enter precharge after t <sub>DPL</sub>	
	L	H	H	H	x	NOP	Nop → Enter precharge after t <sub>DPL</sub>	
	L	H	H	L	x	BST	Nop → Enter precharge after t <sub>DPL</sub>	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	4, 9
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	4
	L	L	H	H	BA, RA	ACT	ILLEGAL	4
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	4
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Refreshing	H	x	x	x	x	DESL	Nop → Enter idle after t <sub>RC</sub>	
	L	H	H	x	x	NOP/BST	Nop → Enter idle after t <sub>RC</sub>	
	L	H	L	x	x	READ/WRIT	ILLEGAL	
	L	L	H	x	x	ACT/PRE/PALL	ILLEGAL	
	L	L	L	x	x	REF/SELF/MRS	ILLEGAL	
Mode register accessing	H	x	x	x	x	DESL	Nop → Enter idle after 2 Clocks	
	L	H	H	H	x	NOP	Nop → Enter idle after 2 Clocks	
	L	H	H	L	x	BST	ILLEGAL	
	L	H	L	x	x	READ/WRITE	ILLEGAL	
	L	L	x	x	x	ACT/PRE/PALL/ REF/SELF/MRS	ILLEGAL	

- Notes
1. H: High level, L: Low level, x: High or Low level (Don't care), V: Valid data input
  2. All entries assume that CKE was active (High level) during the preceding clock cycle.
  3. If both banks are idle, and CKE is inactive (Low level), μPD4516xxx will enter Power down mode. All input buffers except CKE will be disabled.
  4. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
  5. If both banks are idle, and CKE is inactive (Low level), μPD4516xxx will enter Self refresh mode. All input buffers except CKE will be disabled.
  6. Illegal if t<sub>RCD</sub> is not satisfied.
  7. Illegal if t<sub>RAS</sub> is not satisfied.
  8. Must satisfy burst interrupt condition.
  9. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
  10. Must mask preceding data which don't satisfy t<sub>DPL</sub>.
  11. Illegal if t<sub>RRD</sub> is not satisfied.

4.5 Command Truth Table for CKE<sup>Note 1</sup>

Current state	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Action	Notes
Self refresh (S.R.)	H	x	x	x	x	x	x	INVALID, CLK(n-1) would exit S.R.	
	L	H	H	x	x	x	x	S.R. Recovery	2
	L	H	L	H	H	x	x	S.R. Recovery	2
	L	H	L	H	L	x	x	ILLEGAL	2
	L	H	L	L	x	x	x	ILLEGAL	2
	L	L	x	x	x	x	x	Maintain S.R.	
Self refresh recovery	H	H	H	x	x	x	x	Idle after $t_{RC}$	
	H	H	L	H	H	x	x	Idle after $t_{RC}$	
	H	H	L	H	L	x	x	ILLEGAL	
	H	H	L	L	x	x	x	ILLEGAL	
	H	L	H	x	x	x	x	Begin clock suspend next cycle	5
	H	L	L	H	H	x	x	Begin clock suspend next cycle	5
	H	L	L	H	L	x	x	ILLEGAL	
	H	L	L	L	x	x	x	ILLEGAL	
	L	H	x	x	x	x	x	Exit clock suspend next cycle	2
L	L	x	x	x	x	x	Maintain clock suspend		
Power down (P.D.)	H	x	x	x	x	x		INVALID, CLK(n-1) would exit P.D.	
	L	H	x	x	x	x	x	EXIT P.D. → Idle	2
	L	L	x	x	x	x	x	Maintain power down mode	
Both banks idle	H	H	H	x	x	x		Refer to operations in Operative Command Table	
	H	H	L	H	x	x		Refer to operations in Operative Command Table	
	H	H	L	L	H	x		Refer to operations in Operative Command Table	
	H	H	L	L	L	H	x	Refresh	
	H	H	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	H	L	H	x	x	x		Refer to operations in Operative Command Table	
	H	L	L	H	x	x		Refer to operations in Operative Command Table	
	H	L	L	L	H	x		Refer to operations in Operative Command Table	
	H	L	L	L	L	H	x	Self refresh	3
	H	L	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	L	x	x	x	x	x	x	Power down	3
Any state other than listed above	H	H	x	x	x	x	x	Refer to operations in Operative Command Table	
	H	L	x	x	x	x	x	Begin clock suspend next cycle	4
	L	H	x	x	x	x	x	Exit clock suspend next cycle	
	L	L	x	x	x	x	x	Maintain clock suspend	

- Notes
1. H: High level, L: Low level, X: High or low level (Don't care)
  2. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
  3. Power down and Self refresh can be entered only from the both banks idle state.
  4. Must be legal command as defined in Operative Command Table.
  5. Illegal if  $t_{SREX}$  is not satisfied.

4.6 Command Truth Table for Two Banks Operation

CS	RAS	CAS	WE	BA	A10	A9 - A0	Action	"FROM" State	"TO" State
H	x	x	x	x	x	x	NOP	Any	Any
L	H	H	H	x	x	x	NOP	Any	Any
L	H	H	L	x	x	x	BST	(R/W/A)0(I/A)1	A0(I/A)1
								I0(I/A)1	I0(I/A)1
								(R/W/A)1(I/A)0	A1(I/A)0
								I1(I/A)0	I1(I/A)0
L	H	L	H	H	H	CA	Read	(R/W/A)1(I/A)0	RP1(I/A)0
				H	H	CA		A1(R/W)0	RP1A0
				H	L	CA		(R/W/A)1(I/A)0	R1(I/A)0
				H	L	CA		A1(R/W)0	R1A0
				L	H	CA		(R/W/A)0(I/A)1	RP0(I/A)1
				L	H	CA		A0(R/W)1	RP0A1
				L	L	CA		(R/W/A)0(I/A)1	R0(I/A)1
				L	L	CA		A0(R/W)1	R0A1
L	H	L	L	H	H	CA	Write	(R/W/A)1(I/A)0	WP1(I/A)0
				H	H	CA		A1(R/W)0	WP1A0
				H	L	CA		(R/W/A)1(I/A)0	W1(I/A)0
				H	L	CA		A1(R/W)0	W1A0
				L	H	CA		(R/W/A)0(I/A)1	WP0(I/A)1
				L	H	CA		A0(R/W)1	WP0A1
				L	L	CA		(R/W/A)0(I/A)1	W0(I/A)1
				L	L	CA		A0(R/W)1	W0A1
L	L	H	H	H	RA		Activate Row	I1Any0	A1Any0
				L	RA			I0Any1	A0Any1
L	L	H	L	x	H	x	Precharge	(R/W/A/I)0(I/A)1	I0I1
				x	H	x		(R/W/A/I)1(I/A)0	I1I0
				H	L	x		(R/W/A/I)1(I/A)0	I1(I/A)0
				H	L	x		(I/A)1(R/W/A/I)0	I1(R/W/A/I)0
				L	L	x		(R/W/A/I)0(I/A)1	I0(I/A)1
				L	L	x		(I/A)0(R/W/A/I)1	I0(R/W/A/I)1
L	L	L	H	x	x	x	Refresh	I0I1	I0I1
L	L	L	L	Op-Code			Mode Register Access	I0I1	I0I1

Notes 1. Logic level abbreviations

H: High level, L: Low level, x: High or low level (Don't care)

Pin name abbreviation

BA: Bank address (A11)

## 2. State abbreviations

I = Idle

A = Row active

R = Read with No precharge (No precharge is posted)

W = Write with No precharge (No precharge is posted)

RP = Read with auto precharge (Precharge is posted)

WP = Write with auto precharge (Precharge is posted)

Any = Any State

X0Y1 = Y1X0 = Bank0 is in state "X", Bank1 is in state "Y"

(X/Y)0Z1 = Z1(X/Y)0 = Bank0 is in state "X" or "Y", Bank1 is in state "Z"

3. If the  $\mu$ PD4516xxx is in a state other than above listed in the "From State" column, the command is illegal.
4. The states listed under "To" might not be entered on the next clock cycle.  
Timing restrictions apply.

## 5. Initialization

Synchronous DRAM must be initialized in the power on sequence, like conventional DRAM. Once power has been applied, a 100  $\mu$ s delay must precede any signals being toggled.

During this delay, CKE and DQM must be held high.

After the 100  $\mu$ s delay, both banks must be precharged using the precharge command. Once precharge is completed and the minimum  $t_{RP}$  is satisfied, the mode register can be programmed.

Two clocks after the Mode register set command, two CBR refresh command that satisfy the  $t_{RC}$  on each CBR refresh cycle must be performed.

## 6. Programming the Mode Register

The mode register is programmed by the Mode register set command using address bits A11 through A0 as data inputs. The register retains data until it is reprogrammed or the device loses power.

The mode register has four fields;

Options : A11 through A7  
 $\overline{\text{CAS}}$  latency: A6 through A4  
Wrap type : A3  
Burst length: A2 through A0

Following mode register programming, no command can be asserted before at least two clocks have elapsed.

### $\overline{\text{CAS}}$ Latency

$\overline{\text{CAS}}$  latency is the most critical of the parameters being set. It tells the device how many clocks must elapse before the data will be available. The NEC SDRAM is capable of reconfiguring its internal architecture based on the value of  $\overline{\text{CAS}}$  latency.

The value is determined by the frequency of the clock and the speed grade of the device. The table on page 42 shows the relationship of  $\overline{\text{CAS}}$  latency to the clock period and the speed grade of the device.

### Burst Length

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become high impedance.

The burst length is programmable as 1, 2, 4, 8 or full page.

### Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either "Sequential" or "Interleave". The method chosen will depend on the type of CPU in the system.

Some microprocessor cache system are optimized for sequential addressing and others for interleaved addressing. The table on the page 23 shows the addressing sequence for each burst length using them. Both sequences support bursts of 1, 2, 4 and 8. Additionally, sequential sequence supports the full page length.

7. Mode Register

11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1							

JEDEC Standard Test Set (refresh counter test)

11	10	9	8	7	6	5	4	3	2	1	0
x	x	1	0	0	LTMODE		WT			BL	

Burst Read and Single Write (for Write Through Cache)

11	10	9	8	7	6	5	4	3	2	1	0
			1	0							

Use in future

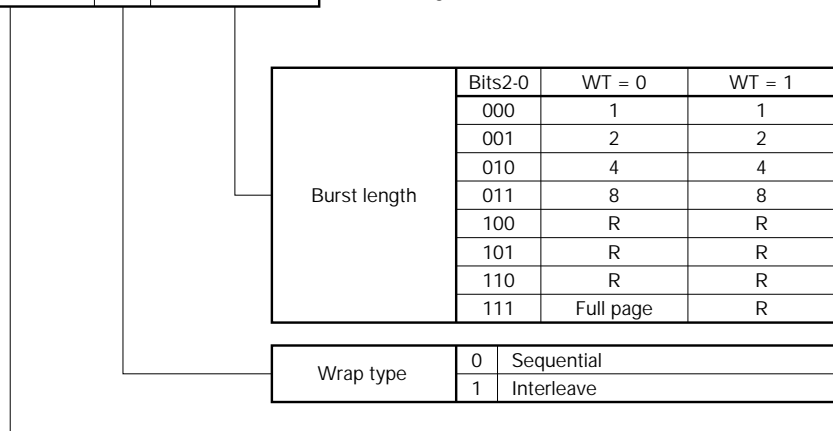
11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	1	1	V	V	V	V	V	V	V

Vender Specific

11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	LTMODE		WT			BL	

Mode Register Set

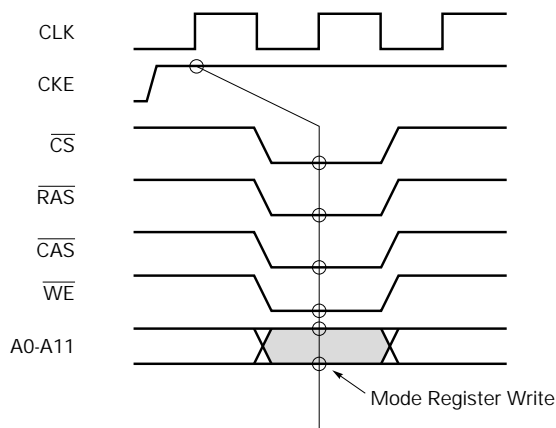
V = Valid  
x = Don't care



Latency mode	Bits6-4	CAS latency
	000	R
	001	1
	010	2
	011	3
	100	R
	101	R
	110	R
111	R	

Remark R: Reserved

Mode Register Write Timing





7.1 Burst Length and Sequence

[Burst of Two]

Starting Address (column address A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

[Burst of Four]

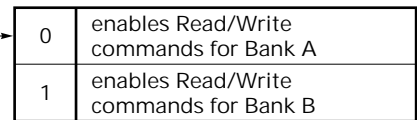
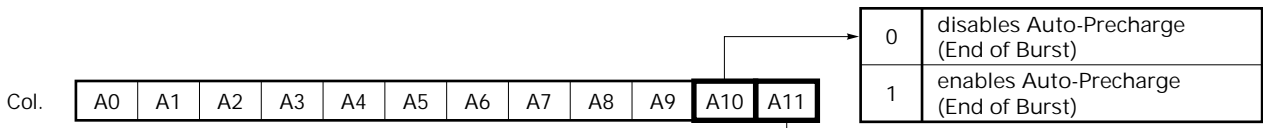
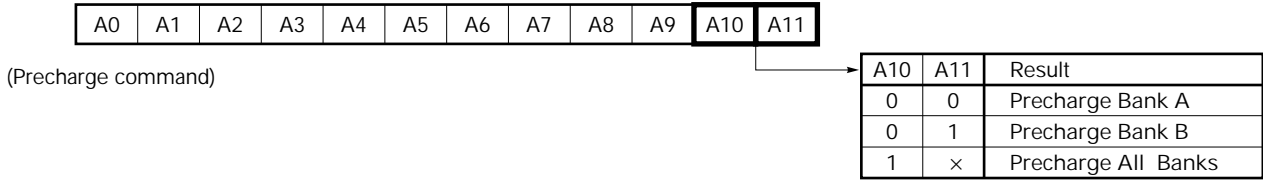
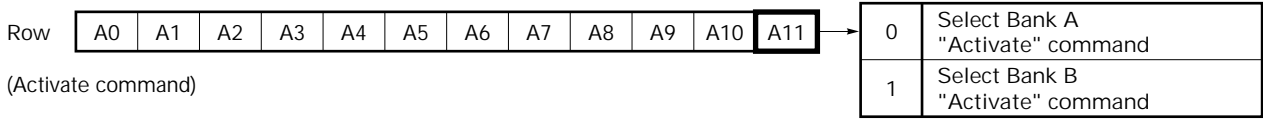
Starting Address (column address A1 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

[Burst of Eight]

Starting Address (column address A2 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Full page burst is an extension of the above tables of Sequential Addressing, with the length being 512 (for 2M ×8 device), 1024 (for 4M ×4 device) and 256 (for 1M ×16 device).

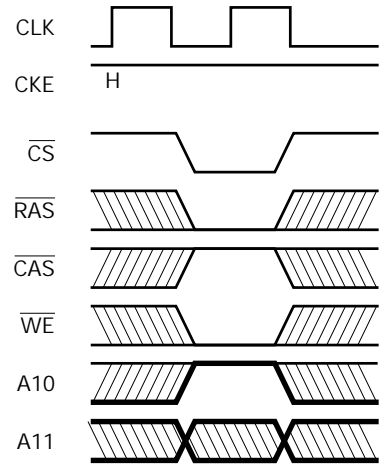
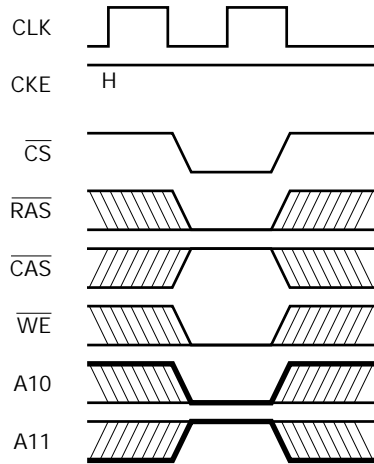
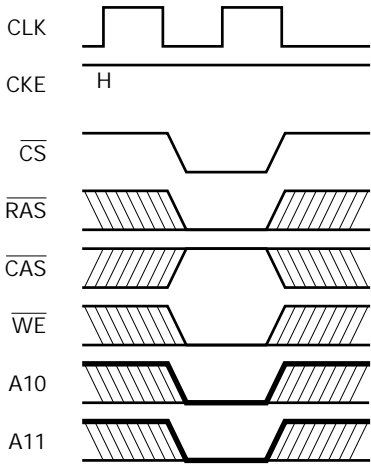
★ 8. Address Bits of Bank-Select and Precharge



Precharge for Bank A

Precharge for Bank B

Precharge for All Banks



9. Auto Precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. A10 high in the read or write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and begins automatically after the burst access.

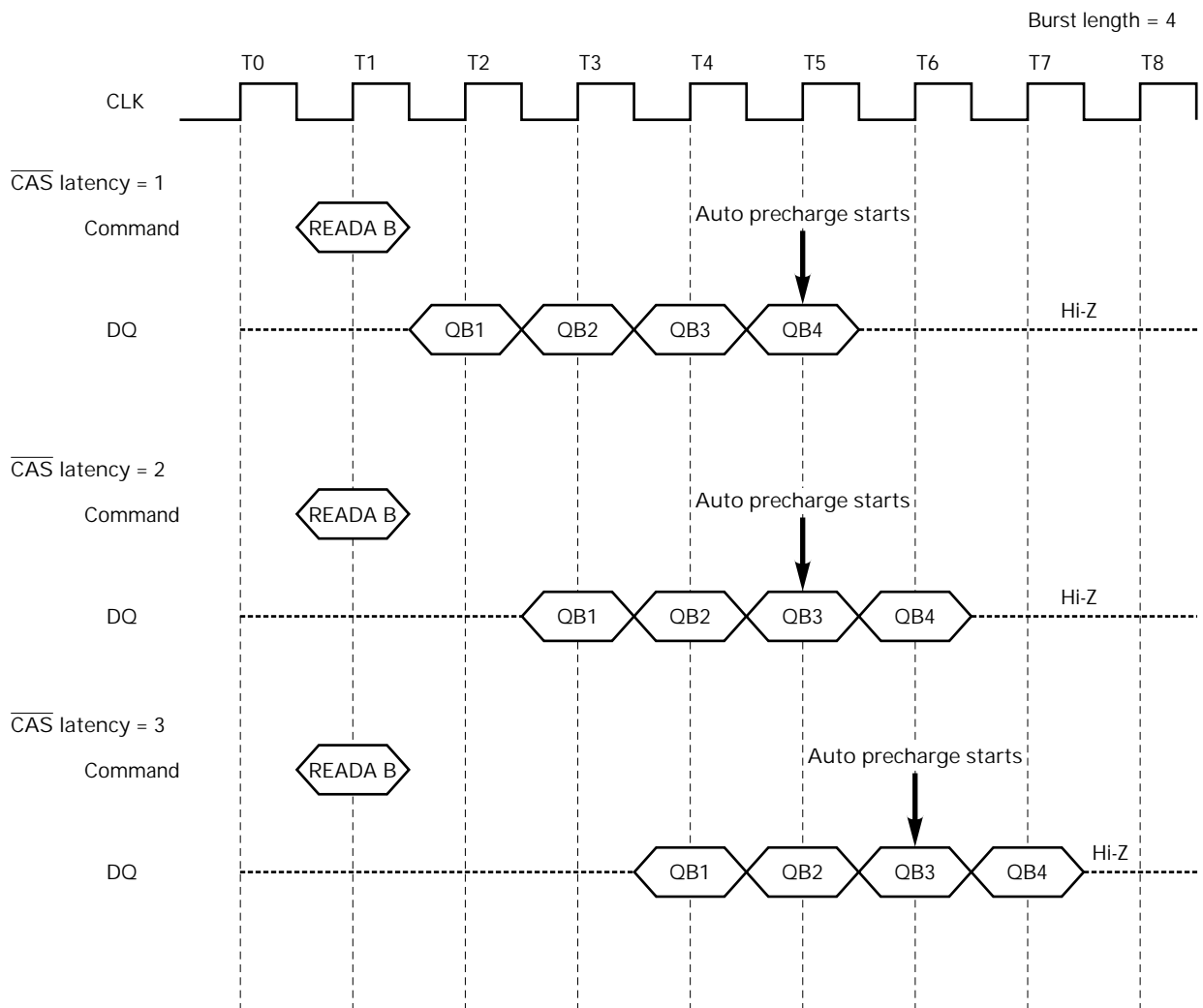
In write cycle, the  $t_{DAL}$  must be satisfied to assert the next activate command to the bank being precharged. It is not necessary to know when the precharge starts.

When using auto precharge in READ cycle, knowing when the precharge starts is important because the next activate command to the bank being precharged cannot be executed until the precharge cycle ends. Once auto precharge has started, an activate command to the bank can be asserted after  $t_{RP}$  has been satisfied.

The clock that begins the auto precharge cycle is depend on both the CAS latency programmed into the mode register and whether READ or WRITE cycle.

9.1 Read with Auto Precharge

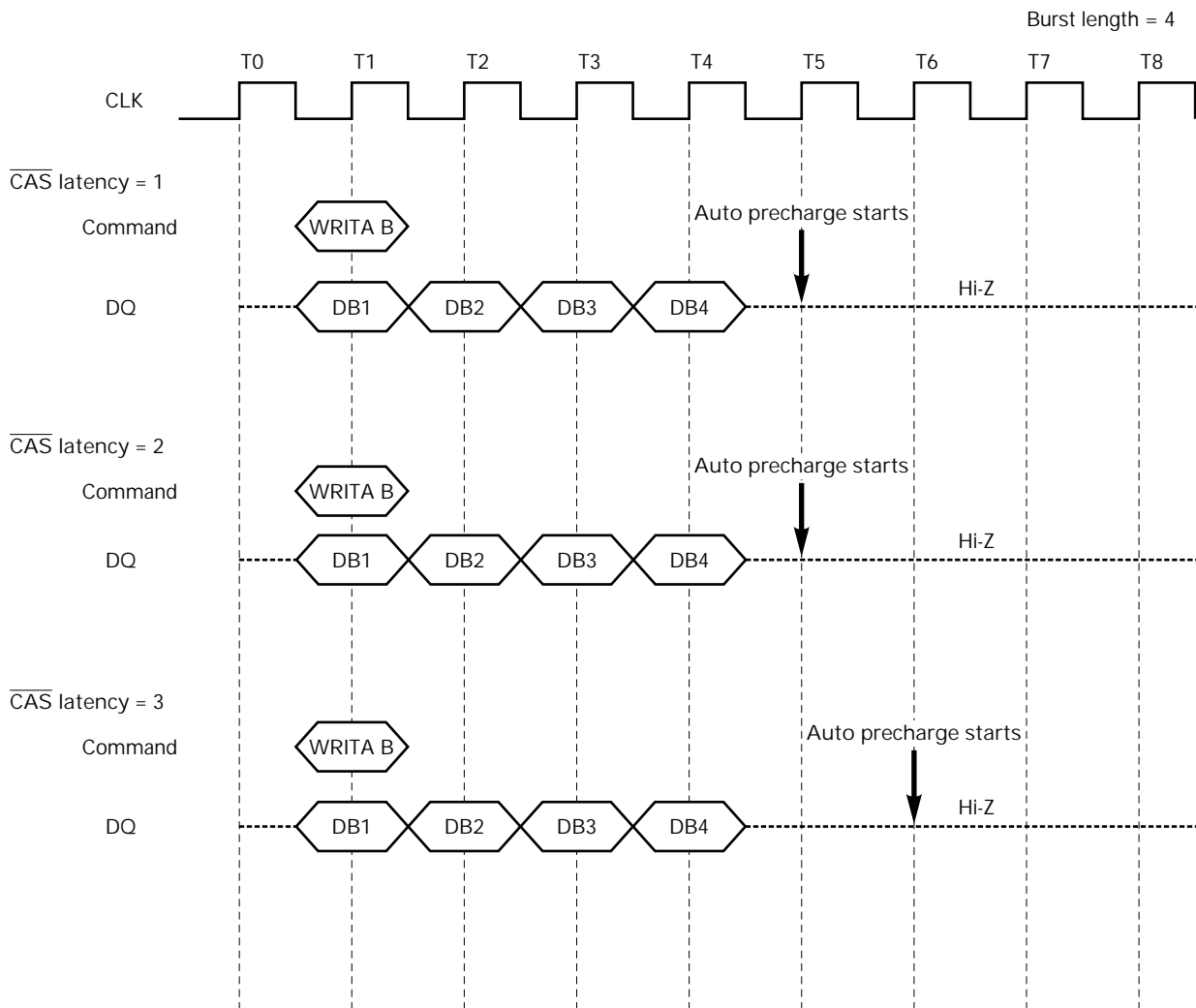
During READ cycle, the auto precharge begins on the clock that indicates the last data word output during the burst is valid ( $\overline{\text{CAS}}$  latency of 1) or one clock earlier ( $\overline{\text{CAS}}$  latency of 2 or 3).



Remark READA means Read with Auto precharge

9.2 Write with Auto Precharge

During WRITE cycle, the auto precharge begins one clock after the last data word input to the device ( $\overline{\text{CAS}}$  latency of 1 or 2) or two clocks after ( $\overline{\text{CAS}}$  latency of 3).



Remark WRITA means Write with Auto precharge

In summary, the auto precharge cycle begins relative to a reference clock that indicates the last data word is valid.

In the table below, minus means clocks before the reference; plus means clocks after the reference.

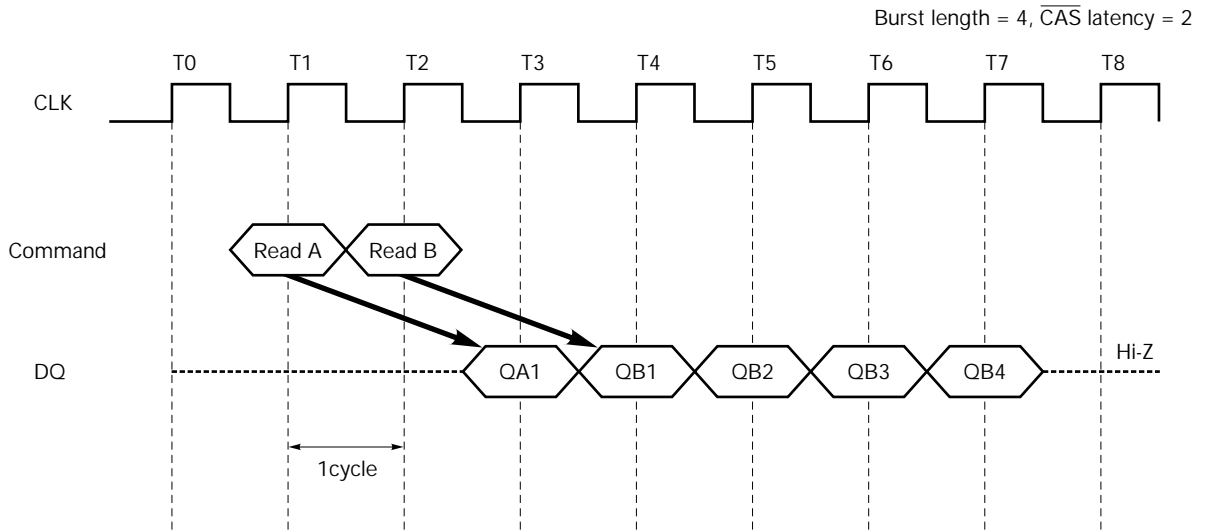
$\overline{\text{CAS}}$ latency	Read	Write
1	0	+1
2	-1	+1
3	-1	+2

10. Read/Write Command Interval

10.1 Read to Read Command Interval

During READ cycle, when new Read command is asserted, it will be effective after  $\overline{\text{CAS}}$  latency, even if the previous READ operation does not completed. READ will be interrupted by another READ.

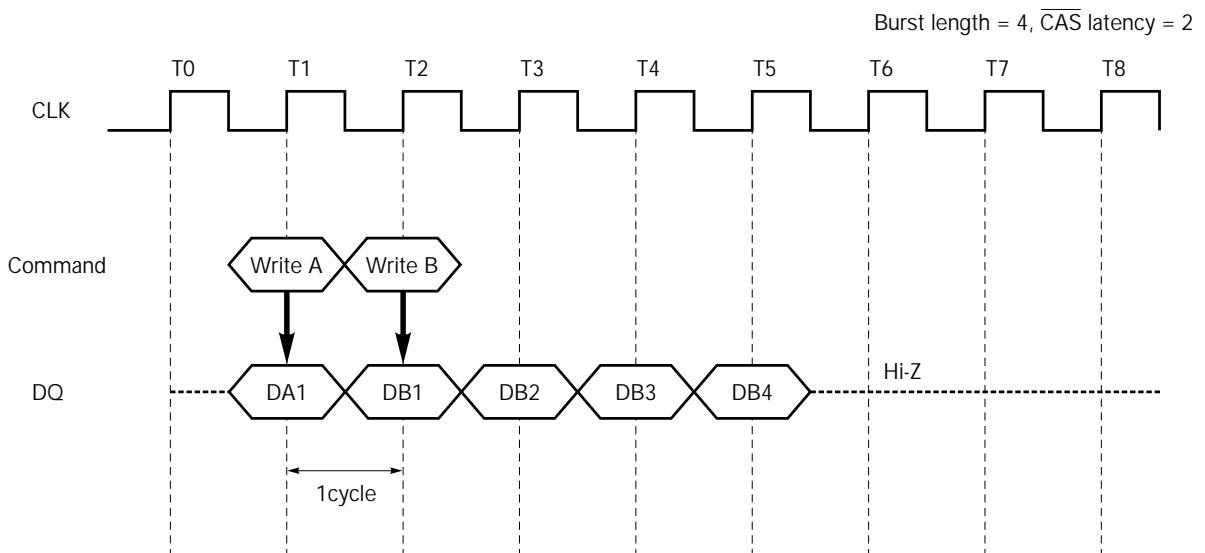
The interval between the commands is 1 cycle minimum. Each Read command can be asserted in every clock without any restriction.



10.2 Write to Write Command Interval

During WRITE cycle, when new Write command is asserted, the previous burst will terminate and the new burst will begin with a new Write command. WRITE will be interrupted by another WRITE.

The interval between the commands is minimum 1. Each Write command can be asserted in every clock without any restriction.

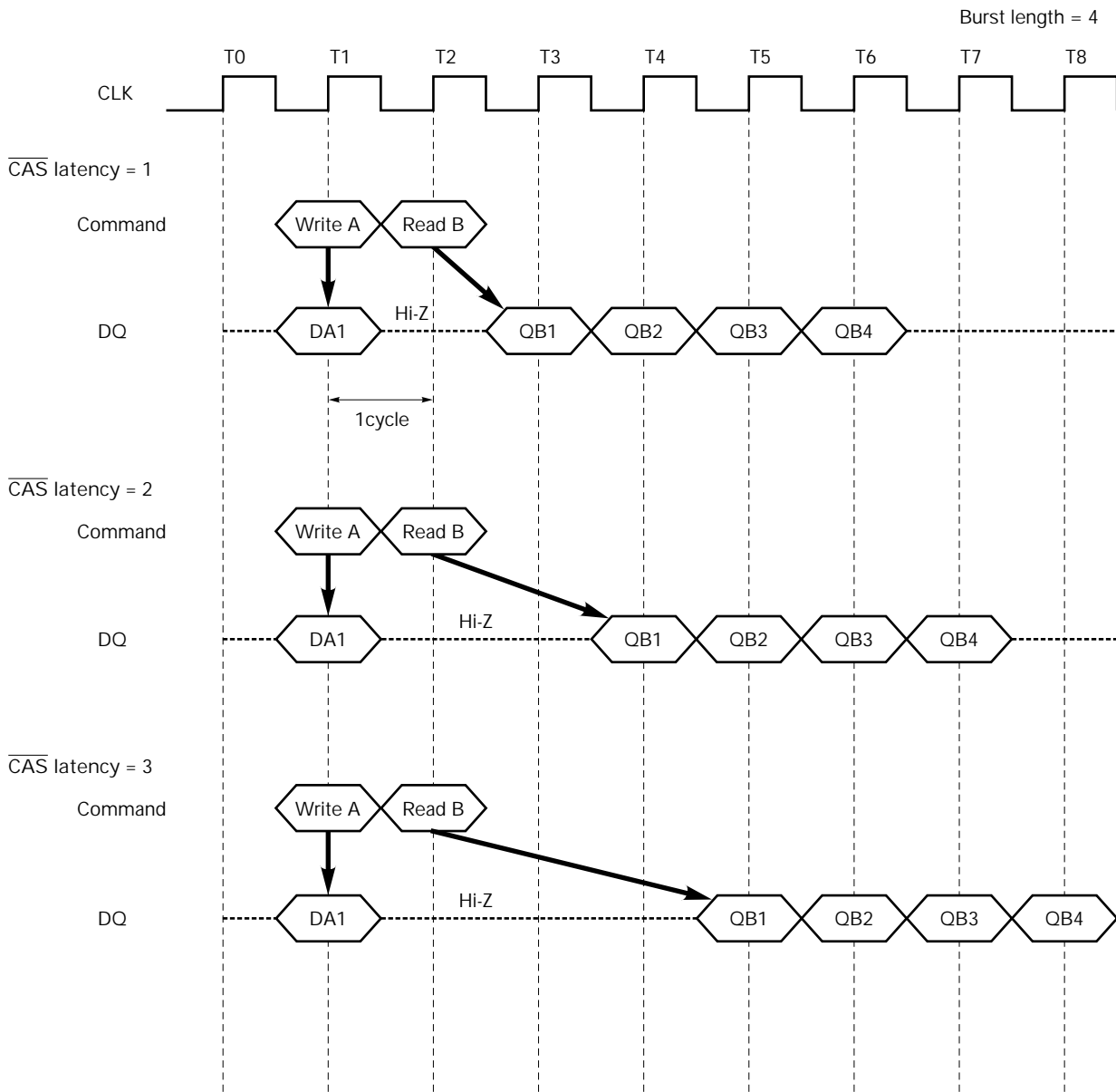


10.3 Write to Read Command Interval

Write command and Read command interval is also 1 cycle.

Only the write data before Read command will be written.

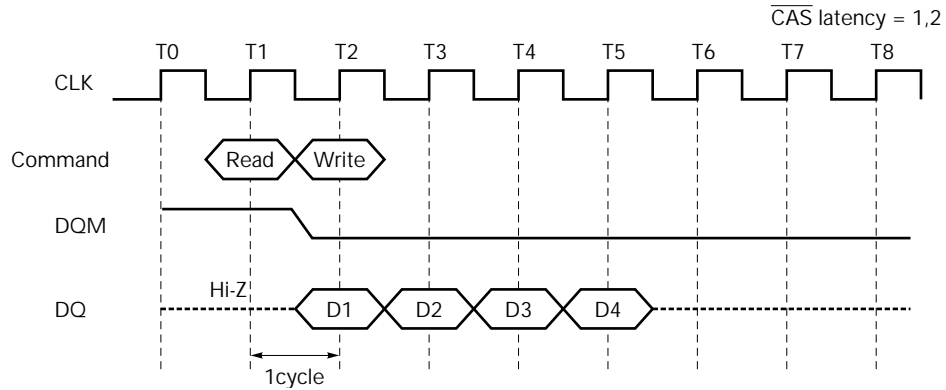
The data bus must be Hi-Z at least one cycle prior to the first DOUT.



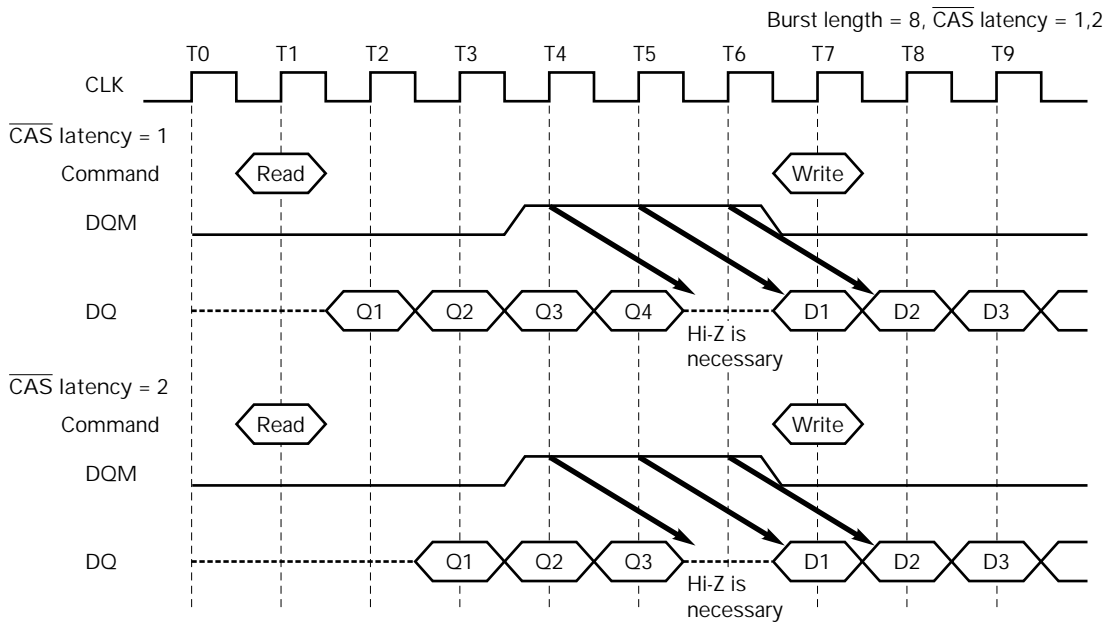
10.4 Read to Write Command Interval

During READ cycle, READ can be interrupted by WRITE. When the  $\overline{\text{CAS}}$  latency is 3 and then the burst length is Full page, the burst read cannot be interrupted by WRITE (A Burst Stop command (BST) or a Precharge command can interrupt).

When the  $\overline{\text{CAS}}$  latency is 1 or 2, the Read and Write command interval is 1 cycle minimum. There is a restriction to avoid data conflict. The data bus must be Hi-Z using DQM before WRITE.

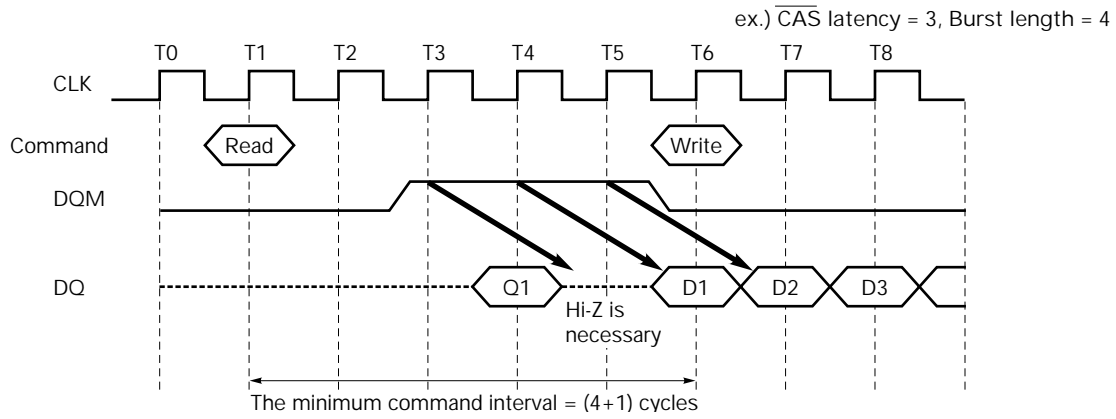


In case  $\overline{\text{CAS}}$  latency is 1 or 2, READ can be interrupted by WRITE. DQM must be High at least 3 clocks prior to the Write command.



In case  $\overline{\text{CAS}}$  latency is 3 (burst length is not Full page), READ can be interrupted by WRITE.

The minimum command interval is [burst length + 1] cycles. DQM must be High at least 3 clocks prior to the Write command.



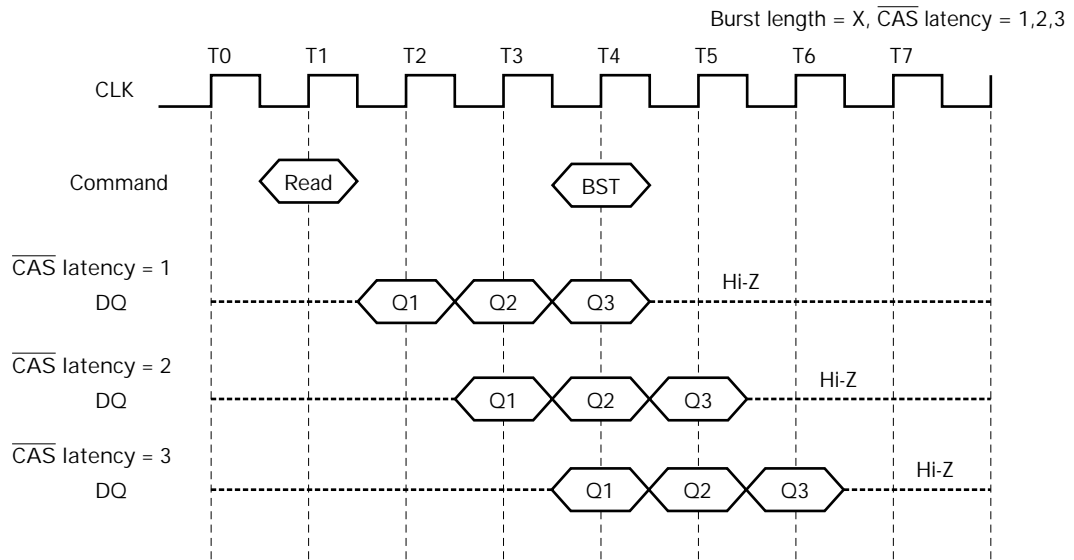


11. Burst Termination

There are two methods to terminate a burst operation other than using a read or a write command. One is the burst stop command and the other is the precharge command.

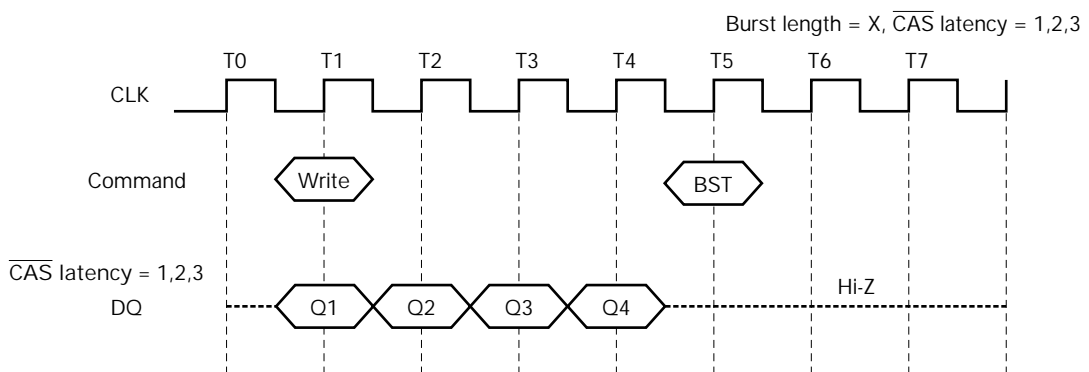
11.1 Burst Stop Command

During READ cycle, when the burst stop command is asserted, the burst read data are terminated and the data bus goes to high-impedance after the  $\overline{\text{CAS}}$  latency from the burst stop command.



Remark BST: Burst stop command

During WRITE cycle, when the burst stop command is asserted, the burst read data are terminated and data bus goes to high-impedance at the same clock with the burst stop command.



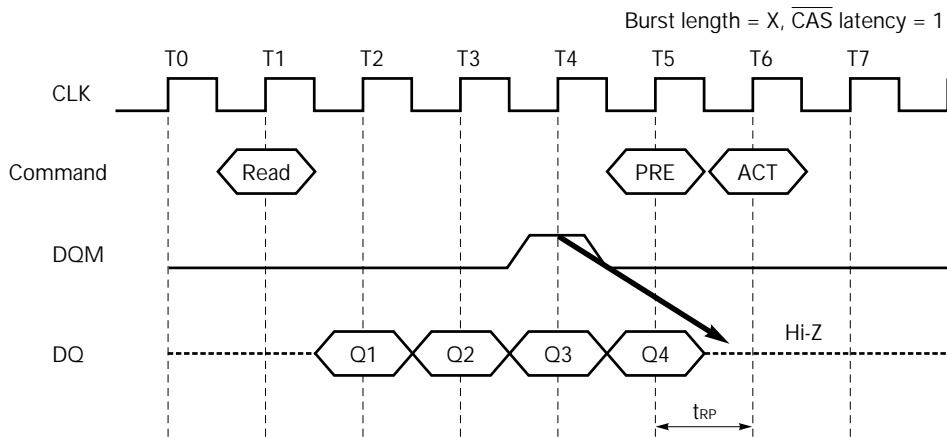
Remark BST: Burst stop command

11.2 Precharge Termination

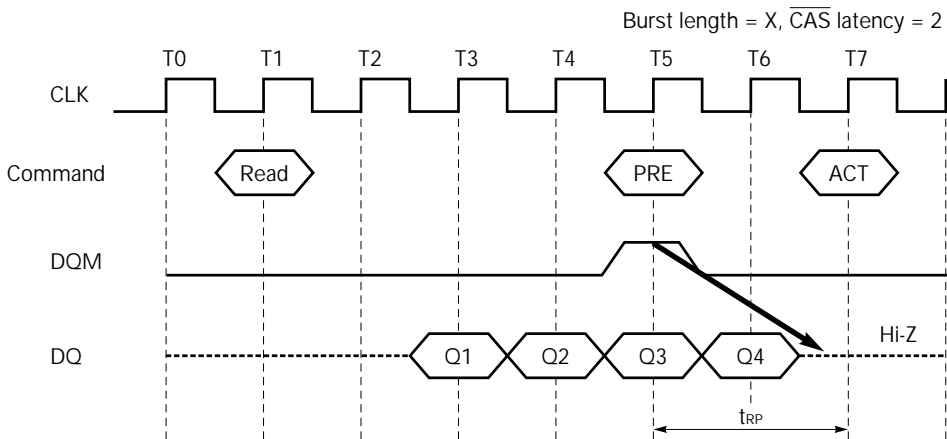
11.2.1 Precharge Termination in READ Cycle

During READ cycle, the burst read operation is terminated by a precharge command. When the precharge command is asserted, the burst read operation is terminated and precharge starts. The same bank can be activated again after  $t_{RP}$  from the precharge command. The DQM must be high to mask the invalid data.

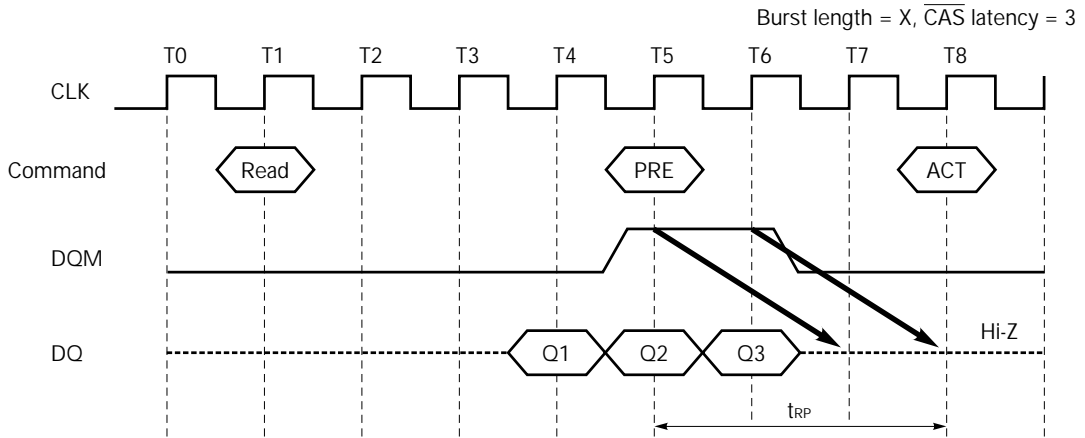
When  $\overline{CAS}$  latency is 1, the read data will remain valid until the precharge command is asserted. Invalid data may appear one clock after valid data out. The DQM may be high to mask the invalid data.



When  $\overline{CAS}$  latency is 2, the read data will remain valid until one clock after the precharge command. Invalid data may appear one clock after valid data out. The DQM may be high to mask the invalid data.



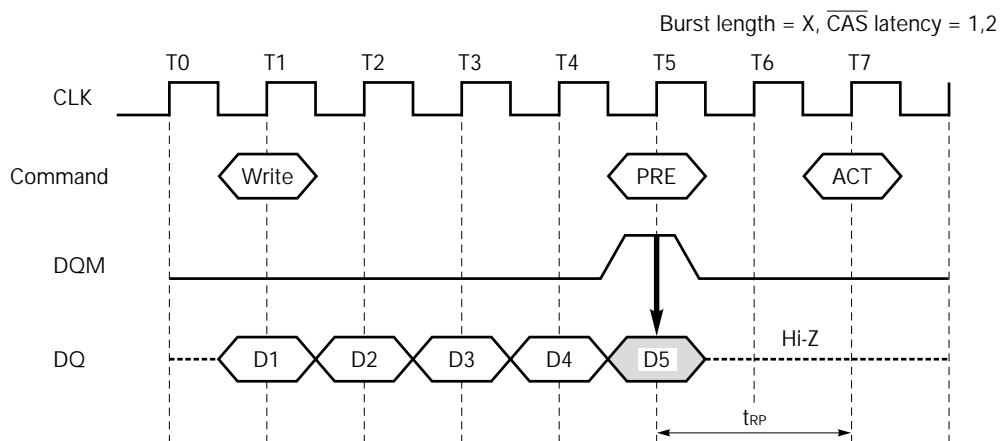
When  $\overline{\text{CAS}}$  latency is 3, the read data will remain valid until one clock after the precharge command. Invalid data may appear one and two clocks after valid data out. The DQM may be high to mask the invalid data.



11.2.2 Precharge Termination in WRITE Cycle

During WRITE cycle, the burst write operation is terminated by a precharge command. When the precharge command is asserted, the burst write operation is terminated and precharge starts. The same bank can be activated again after  $t_{RP}$  from the precharge command. The DQM must be high to mask invalid data in.

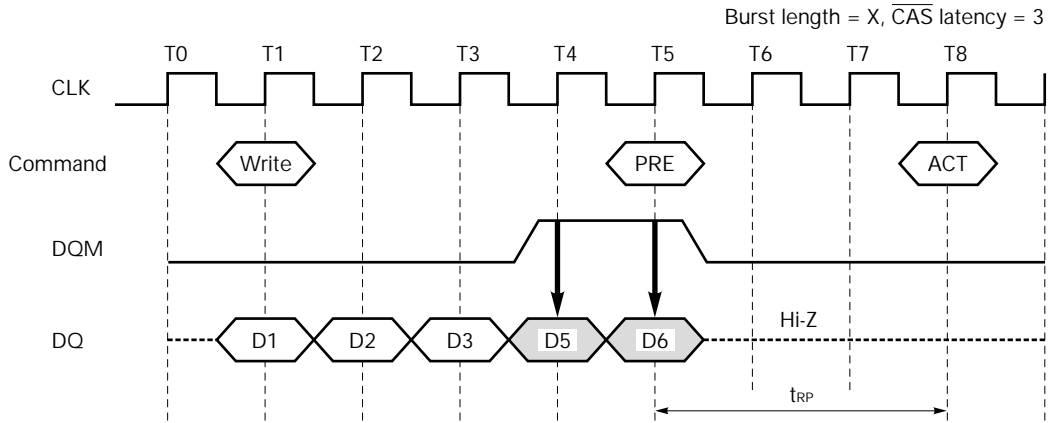
When  $\overline{\text{CAS}}$  latency is 1 or 2, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.



When  $\overline{\text{CAS}}$  latency is 3, the write data written more than one clock prior to the precharge command will be correctly stored.

However, invalid data may be written at one clock before and the same clock as the precharge command.

To prevent this from happening, DQM must be high from one clock prior to the precharge command until the precharge command. This will mask the invalid data.



12. Electrical Specifications (Preliminary)

- All voltage are referenced to V<sub>SS</sub> (GND).
- After power up, wait more than 100 μs and then, execute Power on sequence and Auto Refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V <sub>T</sub>		-1.0 to +4.6	V
Voltage on input pin relative to GND	V <sub>CC</sub> , V <sub>CCQ</sub>		-1.0 to +4.6	V
Short circuit output current	I <sub>o</sub>		50	mA
Power dissipation	P <sub>D</sub>		1	W
Operating ambient temperature	T <sub>A</sub>		0 to +70	°C
Storage temperature	T <sub>stg</sub>		-55 to +125	°C

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V <sub>CC</sub>		3.0	3.3	3.6	V
High level input voltage	V <sub>IH</sub>		2.0		4.6	V
Low level input voltage	V <sub>IL</sub>		-0.3		+0.8	V
Operating ambient temperature	T <sub>A</sub>		0		70	°C

Capacitance (T<sub>A</sub>=25°C, f=1MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>I1</sub>	A0 to A11	2		4	pF
	C <sub>I2</sub>	CLK, CKE, $\overline{CS}$ , RAS, $\overline{CAS}$ , $\overline{WE}$ , DQM, UDQM, LDQM	2		4	pF
Data input/output capacitance	C <sub>I/O</sub>	DQ0 to DQ15	2		5	pF

DC Characteristics 1 (Recommended Operating Conditions unless otherwise noted)

(1/2)

Parameter	Symbol	Test condition	CAS latency	Grade	Maximum			Unit	Notes		
					×4	×8	×16				
Operating current	I <sub>CC1</sub>	Burst length=1 t <sub>RC</sub> ≥ t <sub>RC(MIN.)</sub> I <sub>O</sub> =0mA	CL=1	-10	70	75	80	mA	1		
				-12	65	70	75				
				-13	60	65	70				
				-15	60	65	70				
			CL=2	-10	75	80	85	mA	1		
				-12	70	75	80				
				-13	65	70	75				
				-15	65	70	75				
			CL=3	-10	80	85	90	mA	1		
				-12	75	80	85				
				-13	70	75	80				
				-15	65	70	75				
Precharge standby current in Power down mode	I <sub>CC2P</sub>	CKE ≤ V <sub>IL(MAX.)</sub> t <sub>CK</sub> =15ns			3	3	3	mA			
	I <sub>CC2PS</sub>	CKE ≤ V <sub>IL(MAX.)</sub> t <sub>CK</sub> =∞			2	2	2				
Precharge standby current in Non power down mode	I <sub>CC2N</sub>	CKE ≥ V <sub>IH(MIN.)</sub> t <sub>CK</sub> =15ns CS ≥ V <sub>IH(MIN.)</sub> Input signals are changed one time during 30ns.			20	20	20	mA			
			I <sub>CC2NS</sub>	CKE ≥ V <sub>IH(MIN.)</sub> t <sub>CK</sub> =∞ Input signals are stable.			6			6	6
Active standby current in Power down mode	I <sub>CC3P</sub>	CKE ≤ V <sub>IL(MAX.)</sub> t <sub>CK</sub> =15ns			3	3	3	mA			
	I <sub>CC3PS</sub>	CKE ≤ V <sub>IL(MAX.)</sub> t <sub>CK</sub> =∞			2	2	2				
Active standby current in Non power down mode	I <sub>CC3N</sub>	CKE ≥ V <sub>IH(MIN.)</sub> t <sub>CK</sub> =15ns CS ≥ V <sub>IH(MIN.)</sub> Input signals are changed one time during 30 ns.			25	25	25	mA			
			I <sub>CC3NS</sub>	CKE ≥ V <sub>IH(MIN.)</sub> t <sub>CK</sub> =∞ Input signals are stable.			10			10	10
Operating current (Burst mode)	I <sub>CC4</sub>	t <sub>CK</sub> ≥ t <sub>CK(MIN.)</sub> I <sub>O</sub> =0mA	CL=1	-10	70	75	90	mA	2		
				-12	60	65	80				
				-13	55	60	75				
				-15	55	60	75				
			CL=2	-10	110	120	150				
				-12	90	100	125				
				-13	85	95	115				
				-15	85	95	115				
			CL=3	-10	150	165	210				
				-12	130	145	180				
				-13	120	130	160				
				-15	100	110	140				

Notes 1. I<sub>CC1</sub> depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I<sub>CC1</sub> is measured on condition that addresses are changed only one time during t<sub>CK(MIN.)</sub>.

2. I<sub>CC4</sub> depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I<sub>CC4</sub> is measured on condition that addresses are changed only one time during t<sub>CK(MIN.)</sub>.

DC Characteristics 1 (Recommended Operating Conditions unless otherwise noted)

(2/2)

Parameter	Symbol	Test condition	CAS latency	Grade	Maximum			Unit	Note
					×4	×8	×16		
Refresh current	I <sub>CC5</sub>	t <sub>RC</sub> ≥ t <sub>RC(MIN.)</sub>	CL=1	-10	90	90	90	mA	1
				-12	80	80	80		
				-13	75	75	75		
				-15	75	75	75		
			CL=2	-10	95	95	95		
				-12	85	85	85		
				-13	80	80	80		
				-15	80	80	80		
			CL=3	-10	100	100	100		
				-12	90	90	90		
				-13	85	85	85		
				-15	80	80	80		
Self refresh Current	I <sub>CC6</sub>	CKE ≤ 0.2V	-**	2	2	2	mA		
			-**L	100	100	100	μA		

Note 1. I<sub>CC5</sub> is measured on condition that addresses are changed only one time during t<sub>CK(MIN.)</sub>.

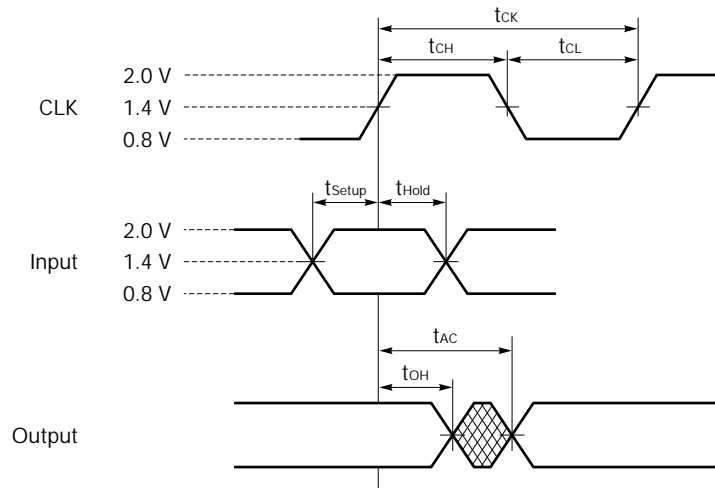
DC Characteristics 2 (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input leakage current	I <sub>I(L)</sub>	V <sub>I</sub> =0 to 3.6V, all other pins not under test =0V	-1.0		+1.0	μA
Output leakage current	I <sub>O(L)</sub>	D <sub>OUT</sub> is disabled, V <sub>O</sub> =0 to 3.6V	-1.0		+1.0	μA
High level output voltage	V <sub>OH</sub>	I <sub>O</sub> =-2mA	2.4			V
Low level output voltage	V <sub>OL</sub>	I <sub>O</sub> =+2mA			0.4	V

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

Test Conditions

- AC measurements assume  $t_T=1ns$ .
- Reference level for measuring timing of input signals is 1.4V. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- If  $t_T$  is longer than 1 ns, reference level for measuring timing of input signals is  $V_{IH(MIN.)}$  and  $V_{IL(MAX.)}$ .
- An access time is measured at 1.4V.



Synchronous Characteristics

(1/2)

★

Parameter	Symbol	-10		-12		-13		-15		Unit	Notes	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
Clock cycle time	$\overline{CAS}$ latency=3	$t_{CK3}$	10	(100MHz)	12	(83MHz)	13	(77MHz)	15	(66MHz)	ns	
	$\overline{CAS}$ latency=2	$t_{CK2}$	15	(66MHz)	18	(55MHz)	19.5	(50MHz)	19.5	(50MHz)	ns	
	$\overline{CAS}$ latency=1	$t_{CK1}$	30	(33MHz)	36	(28MHz)	39	(25MHz)	39	(25MHz)	ns	
Access time from CLK	$\overline{CAS}$ latency=3	$t_{AC3}$		9		11		12		14	ns	1
	$\overline{CAS}$ latency=2	$t_{AC2}$		12		15		16.5		16.5	ns	2
	$\overline{CAS}$ latency=1	$t_{AC1}$		27		33		36		36	ns	2
CLK high level width	$t_{CH}$	3.5		4		5		5		5	ns	
CLK low level width	$t_{CL}$	3.5		4		5		5		5	ns	
Data-out hold time	$t_{OH}$	4		4		4		4		4	ns	
Data-out low-impedance time	$t_{LZ}$	0		0		0		0		0	ns	
Data-out high-impedance time	$t_{HZ}$		10		10		10		10	10	ns	
Data-in setup time	$t_{DS}$	3		3.5		3.5		3.5		3.5	ns	
Data-in hold time	$t_{DH}$	1		1.5		1.5		1.5		1.5	ns	
Address setup time	$t_{AS}$	3		3.5		3.5		3.5		3.5	ns	
Address hold time	$t_{AH}$	1		1.5		1.5		1.5		1.5	ns	
CKE setup time	$t_{CKS}$	3		3.5		3.5		3.5		3.5	ns	
CKE hold time	$t_{CKH}$	1		1.5		1.5		1.5		1.5	ns	
CKE setup time (Power down exit)	$t_{CKSP}$	3		3.5		3.5		3.5		3.5	ns	

★

- Notes 1. Loading capacitance is 50 pF.  
2. Loading capacitance is 80 pF.



Synchronous Characteristics

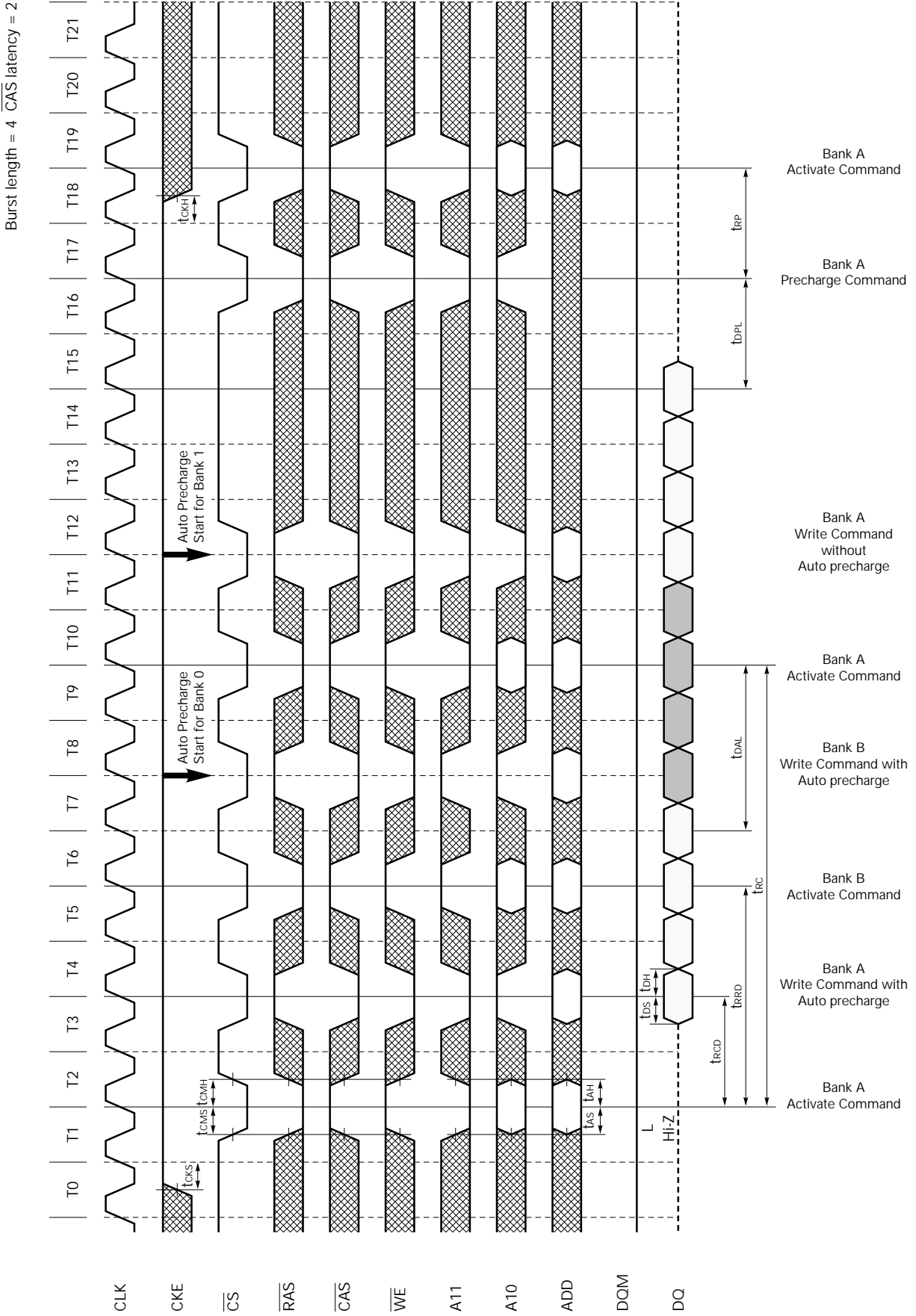
(2/2)

Parameter	Symbol	-10		-12		-13		-15		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Command ( $\overline{CS}$ , $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , DQM) setup time	t <sub>CMS</sub>	3		3.5		3.5		3.5		ns	
Command ( $\overline{CS}$ , $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , DQM) hold time	t <sub>CMH</sub>	1		1.5		1.5		1.5		ns	

Asynchronous Characteristics

Parameter	Symbol	-10		-12		-13		-15		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
REF to REF/ACT Command period	t <sub>RC</sub>	100		120		130		130		ns	
ACT to PRE Command period	t <sub>RAS</sub>	70	120,000	84	120,000	91	120,000	91	120,000	ns	
PRE to ACT Command period	t <sub>RP</sub>	30		36		39		39		ns	
Delay time ACT to READ/ WRITE Command	t <sub>RCD</sub>	30		36		39		39		ns	
ACT(0) to ACT(1) Command period	t <sub>RRD</sub>	30		36		39		39		ns	
Data-in to PRE Command period	$\overline{CAS}$ latency=3 t <sub>DPL3</sub>	1CLK+10		1CLK+12		1CLK+13		1CLK+15		ns	
	$\overline{CAS}$ latency=2 t <sub>DPL2</sub>	15		18		19.5		19.5		ns	
	$\overline{CAS}$ latency=1 t <sub>DPL1</sub>	15		18		19.5		19.5		ns	
Data-in to ACT (REF) Command period (Auto precharge)	$\overline{CAS}$ latency=3 t <sub>DAL3</sub>	2CLK+30		2CLK+36		2CLK+39		2CLK+45		ns	
	$\overline{CAS}$ latency=2 t <sub>DAL2</sub>	1CLK+30		1CLK+36		1CLK+39		1CLK+39		ns	
	$\overline{CAS}$ latency=1 t <sub>DAL1</sub>	1CLK+30		1CLK+36		1CLK+39		1CLK+39		ns	
Self refresh exit time	t <sub>SREX</sub>	20		24		26		26		ns	
Transition time	t <sub>T</sub>	1	30	1	30	1	30	1	30	ns	
Refresh time	t <sub>REF</sub>		32		32		32		32	ms	

12.1 AC Parameters for Write Timing



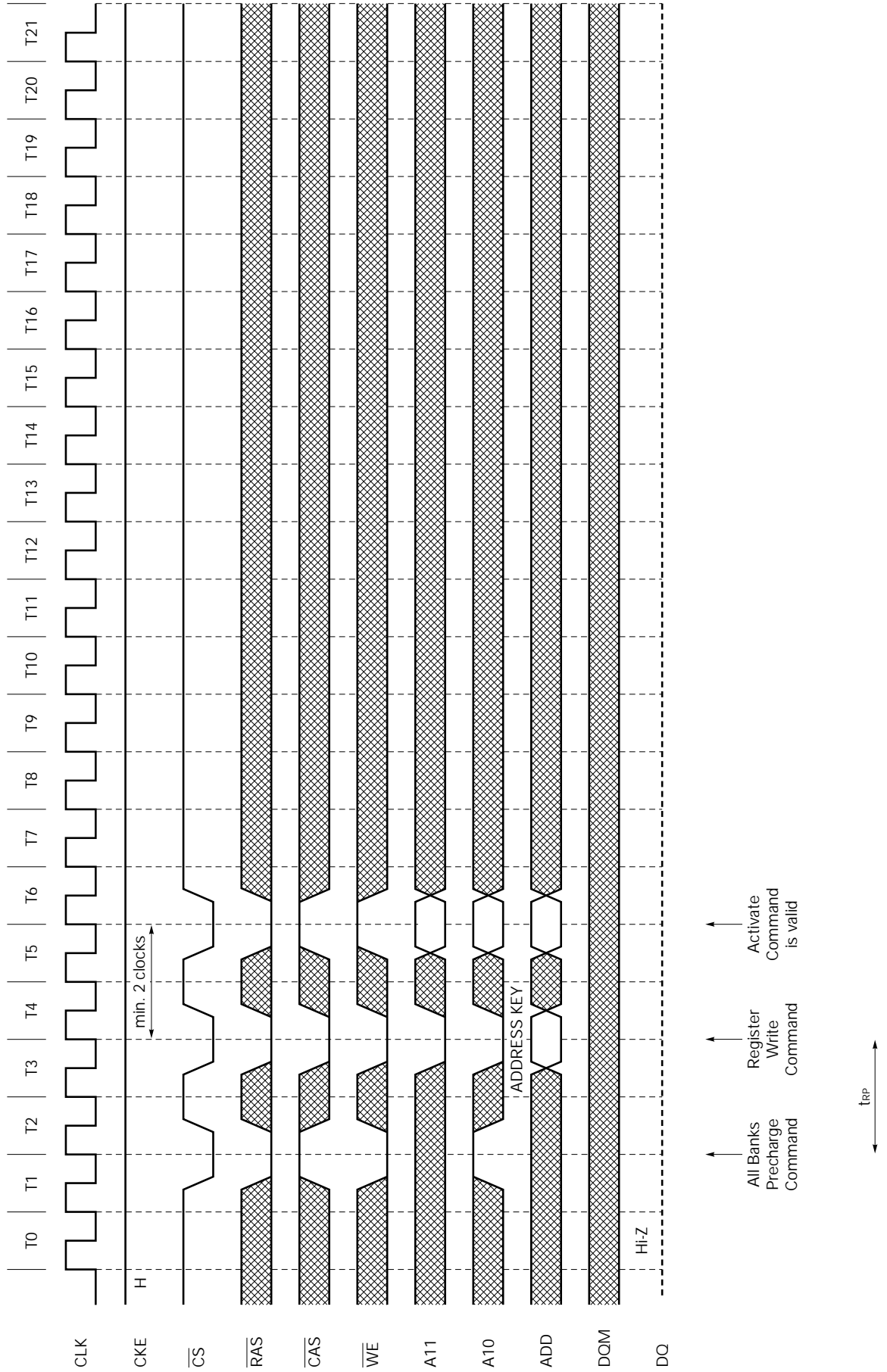


12.3 Relationship between Frequency and Latency

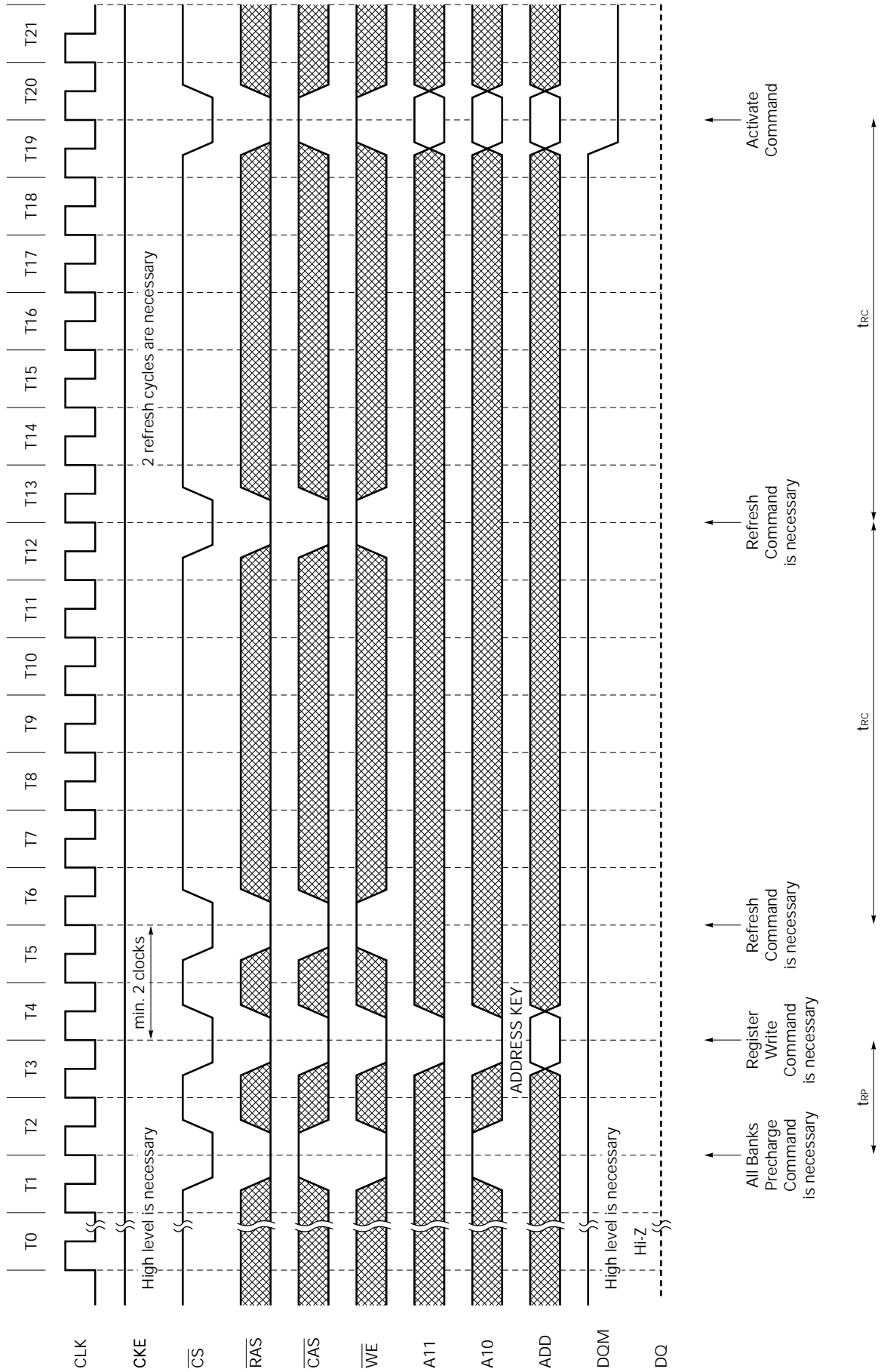
Speed version	-10			-12			-13			-15		
Clock cycle time [ns]	10	15	30	12	18	36	13	19.5	39	15	19.5	39
★ Frequency [MHz]	100	66	33	83	55	28	77	50	25	66	50	25
CAS latency	3	2	1	3	2	1	3	2	1	3	2	1
[t <sub>RC</sub> D]	3	2	1	3	2	1	3	2	1	3	2	1
RAS latency (CAS latency + [t <sub>RC</sub> D])	6	4	2	6	4	2	6	4	2	6	4	2
[t <sub>RC</sub> ]	10	7	4	10	7	4	10	7	4	10	7	4
[t <sub>RA</sub> S]	7	5	3	7	5	3	7	5	3	7	5	3
[t <sub>RR</sub> D]	3	2	1	3	2	1	3	2	1	3	2	1
[t <sub>RP</sub> ]	3	2	1	3	2	1	3	2	1	3	2	1
[t <sub>DPL</sub> ]	2	1	1	2	1	1	2	1	1	2	1	1
[t <sub>DAL</sub> ]	5	3	2	5	3	2	5	3	2	5	3	2
[t <sub>SREX</sub> ]	2	2	1	2	2	1	2	2	1	2	2	1

12.4 Mode Register Write

Burst length = 4  $\overline{\text{CAS}}$  latency = 2



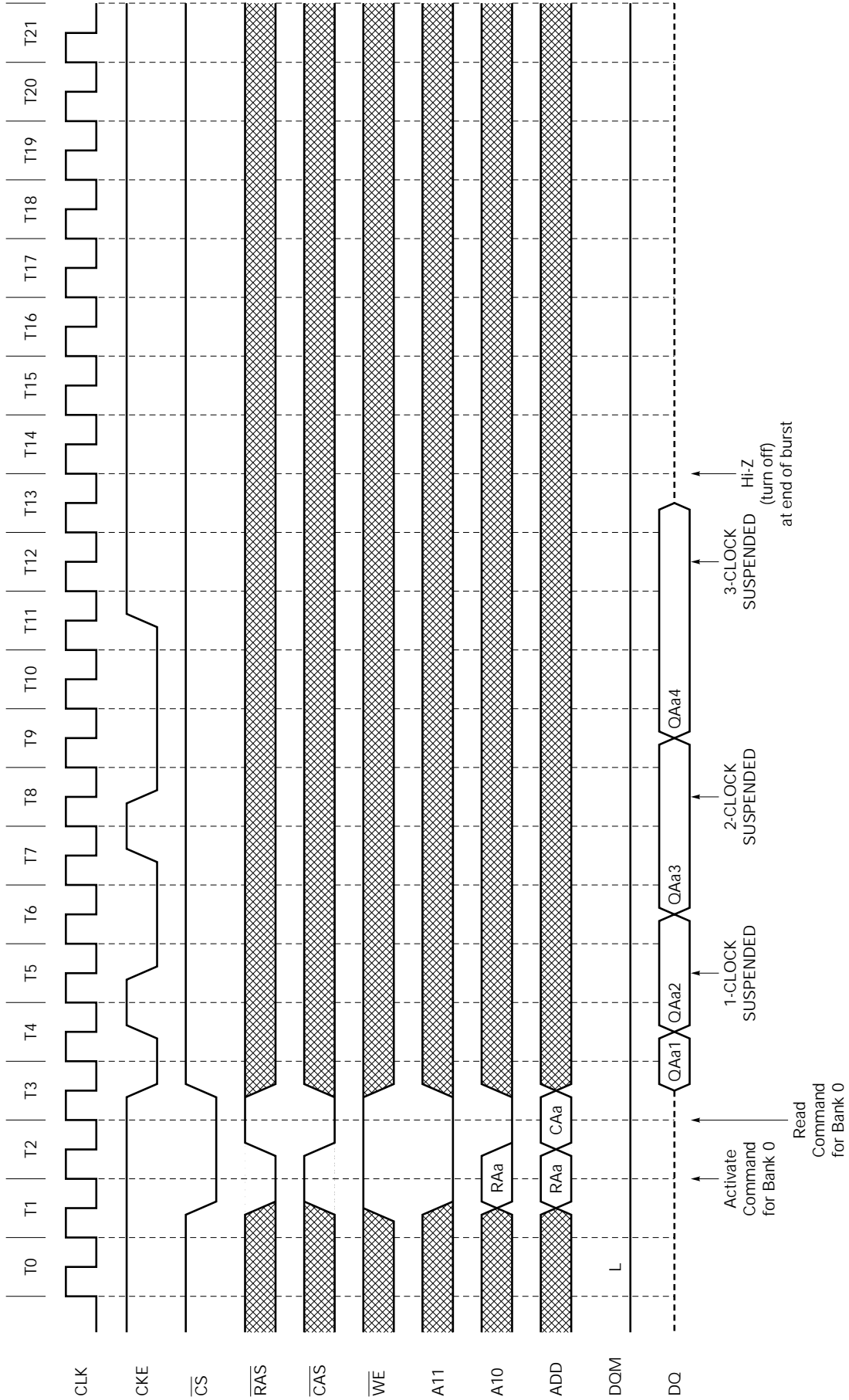
12.5 Power on Sequence and Auto Refresh





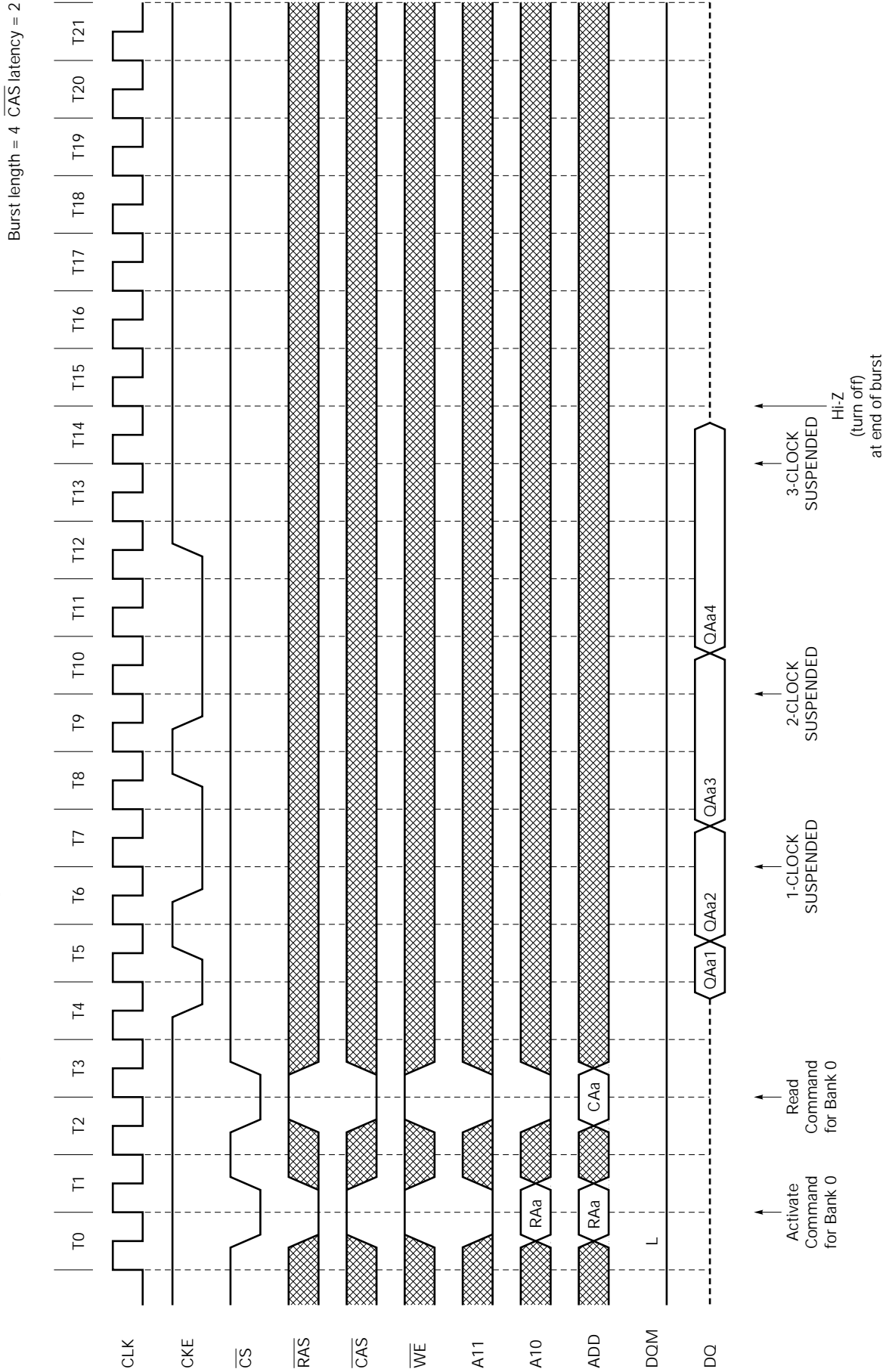
12.7 Clock Suspension during Burst Read (using CKE Function) (1/3)

Burst length = 4 CAS latency = 1



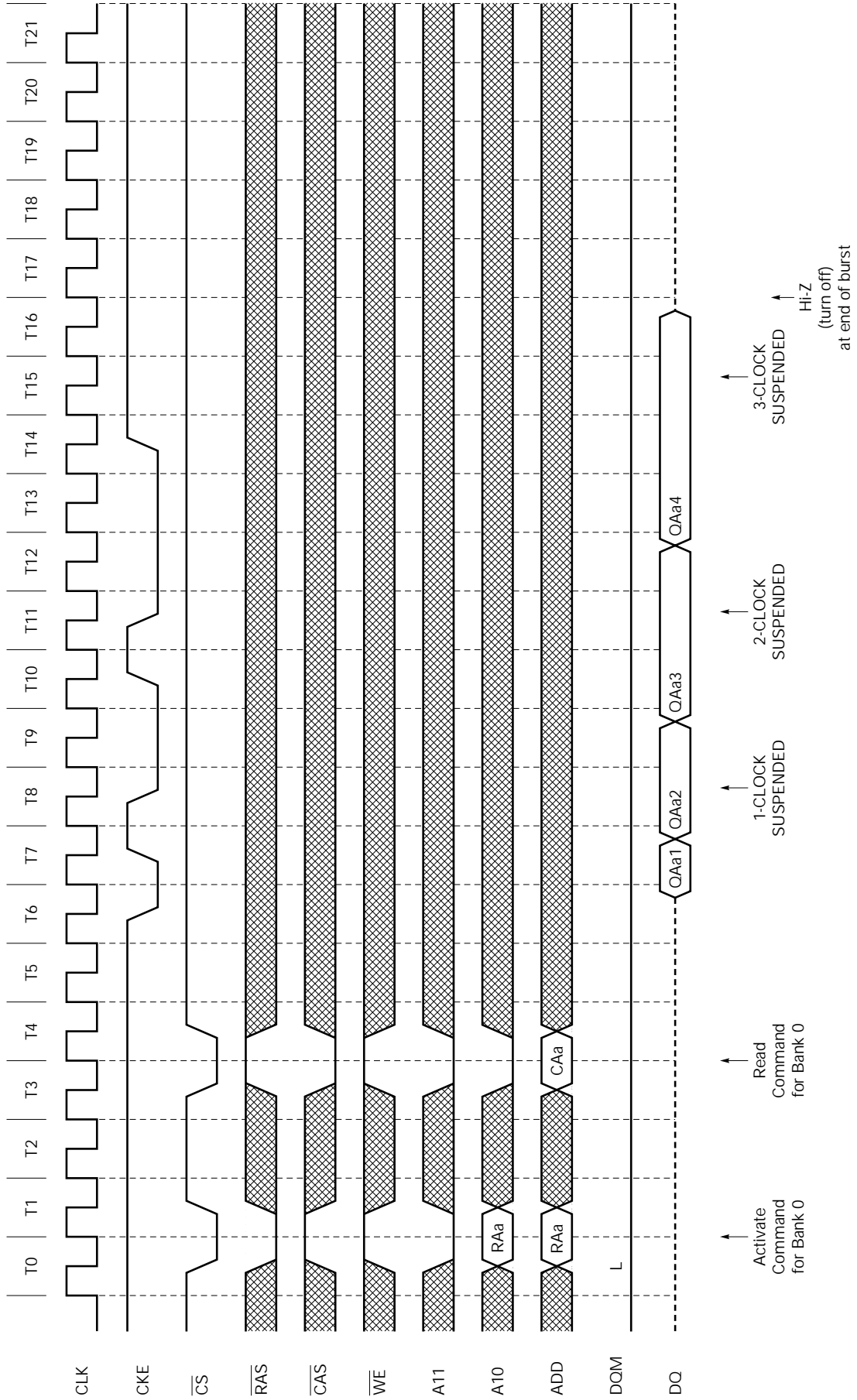


Clock Suspension during Burst Read (using CKE Function) (2/3)

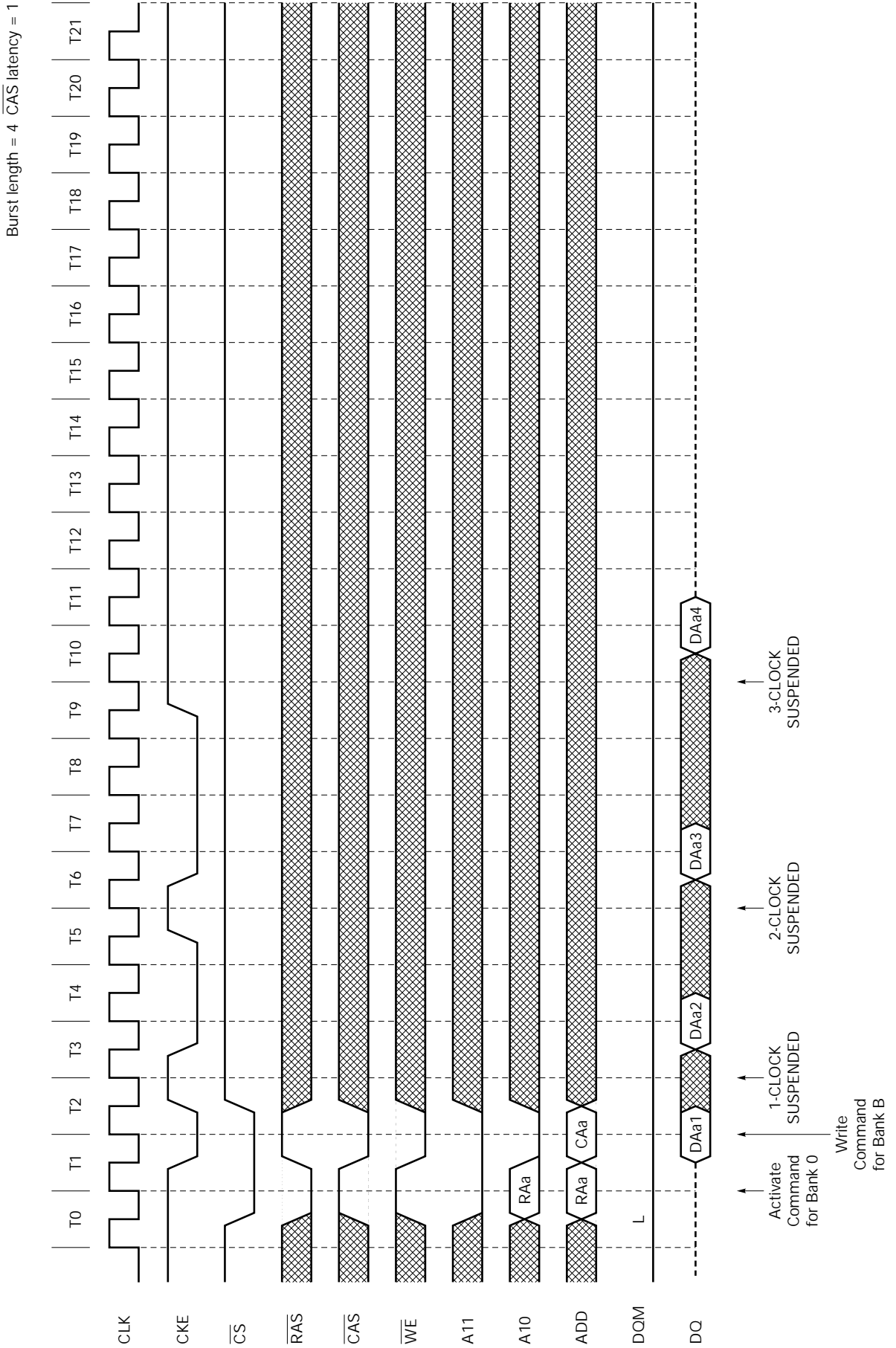


Clock Suspension during Burst Read (using CKE Function) (3/3)

Burst length = 4 CAS latency = 3

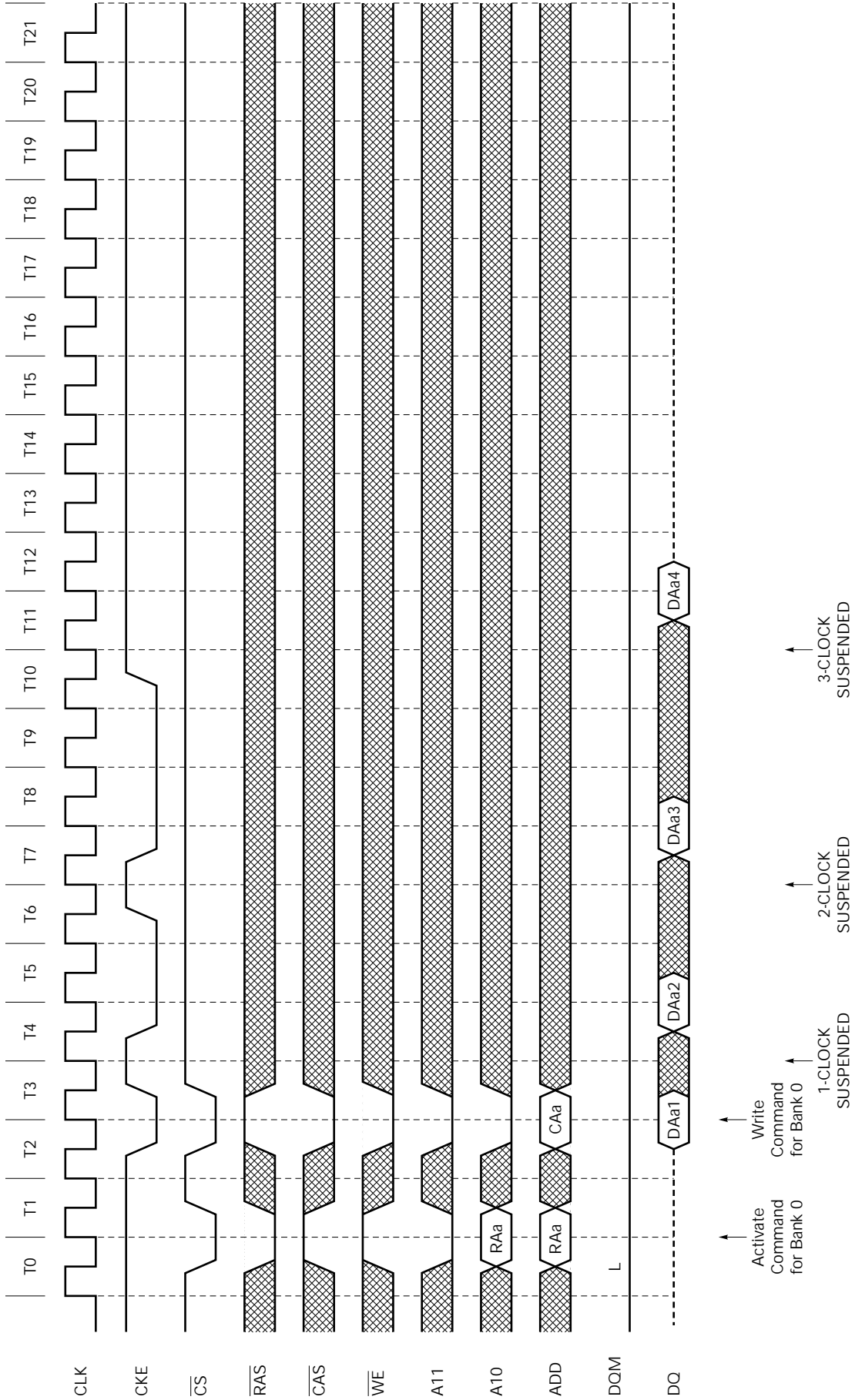


12.8 Clock Suspension during Burst Write (using CKE Function) (1/3)



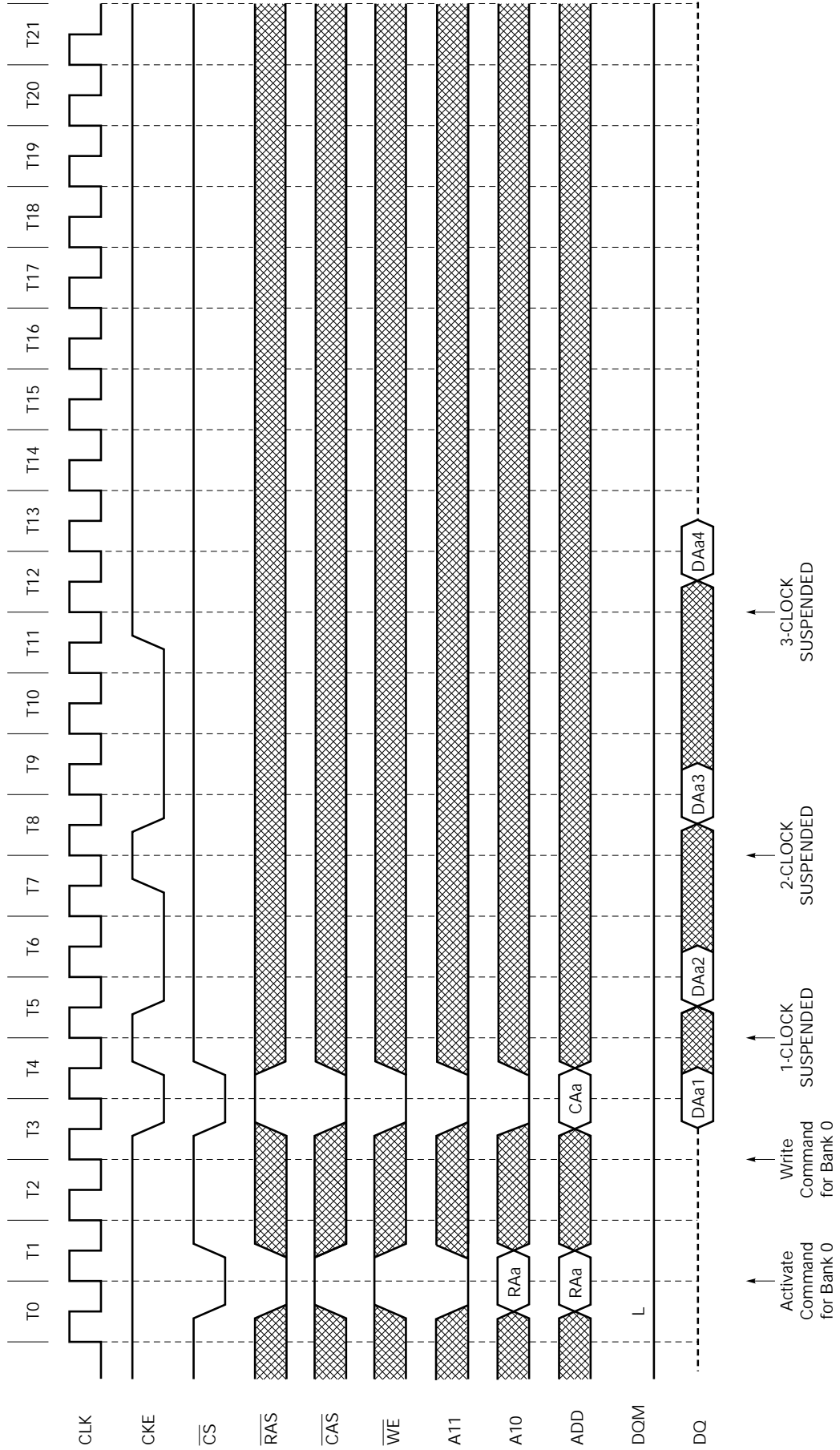
Clock Suspension during Burst Write (using CKE Function) (2/3)

Burst length = 4 CAS latency = 2



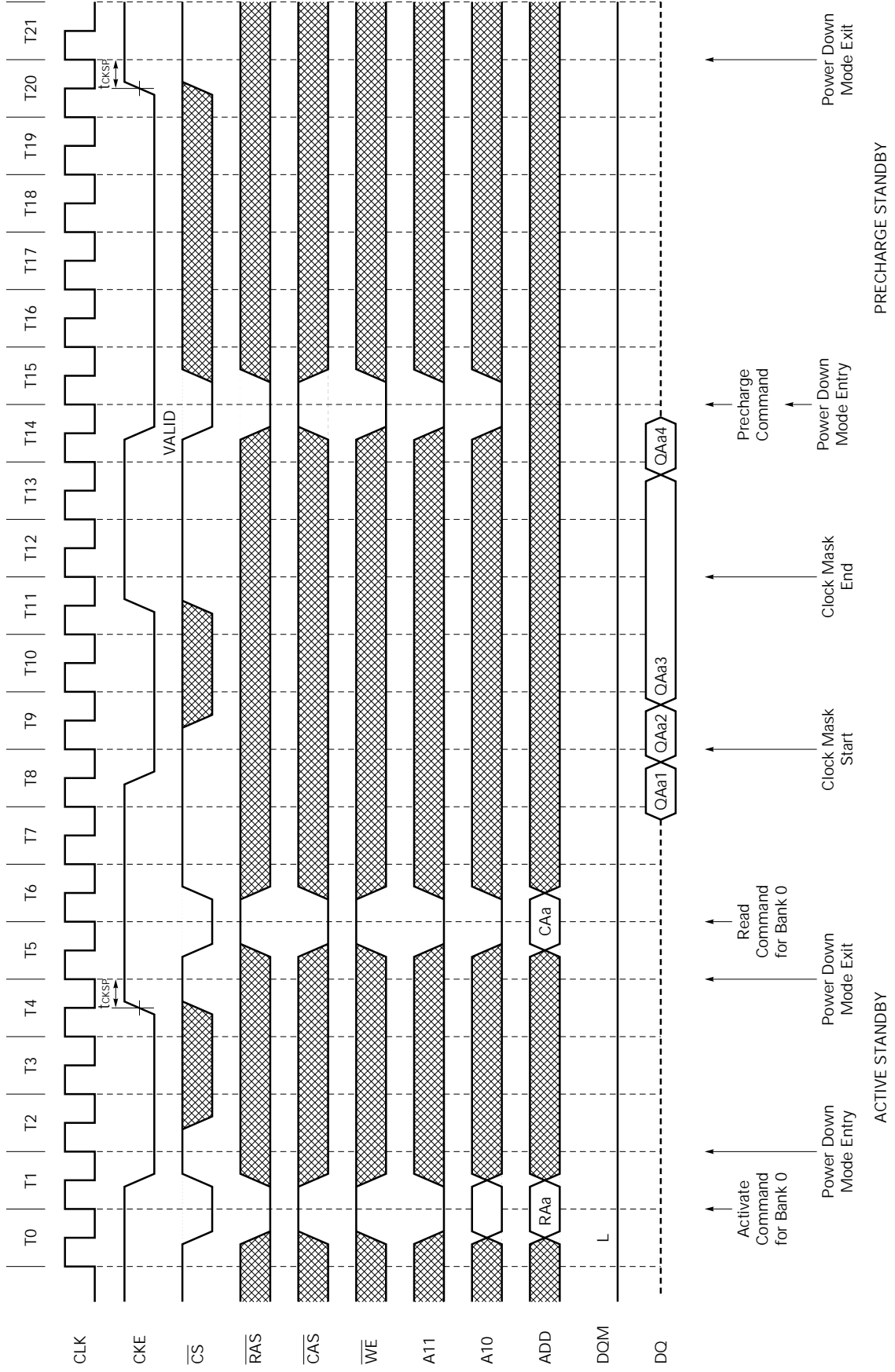
Clock Suspension during Burst Write (using CKE Function) (3/3)

Burst length = 4 CAS latency = 3

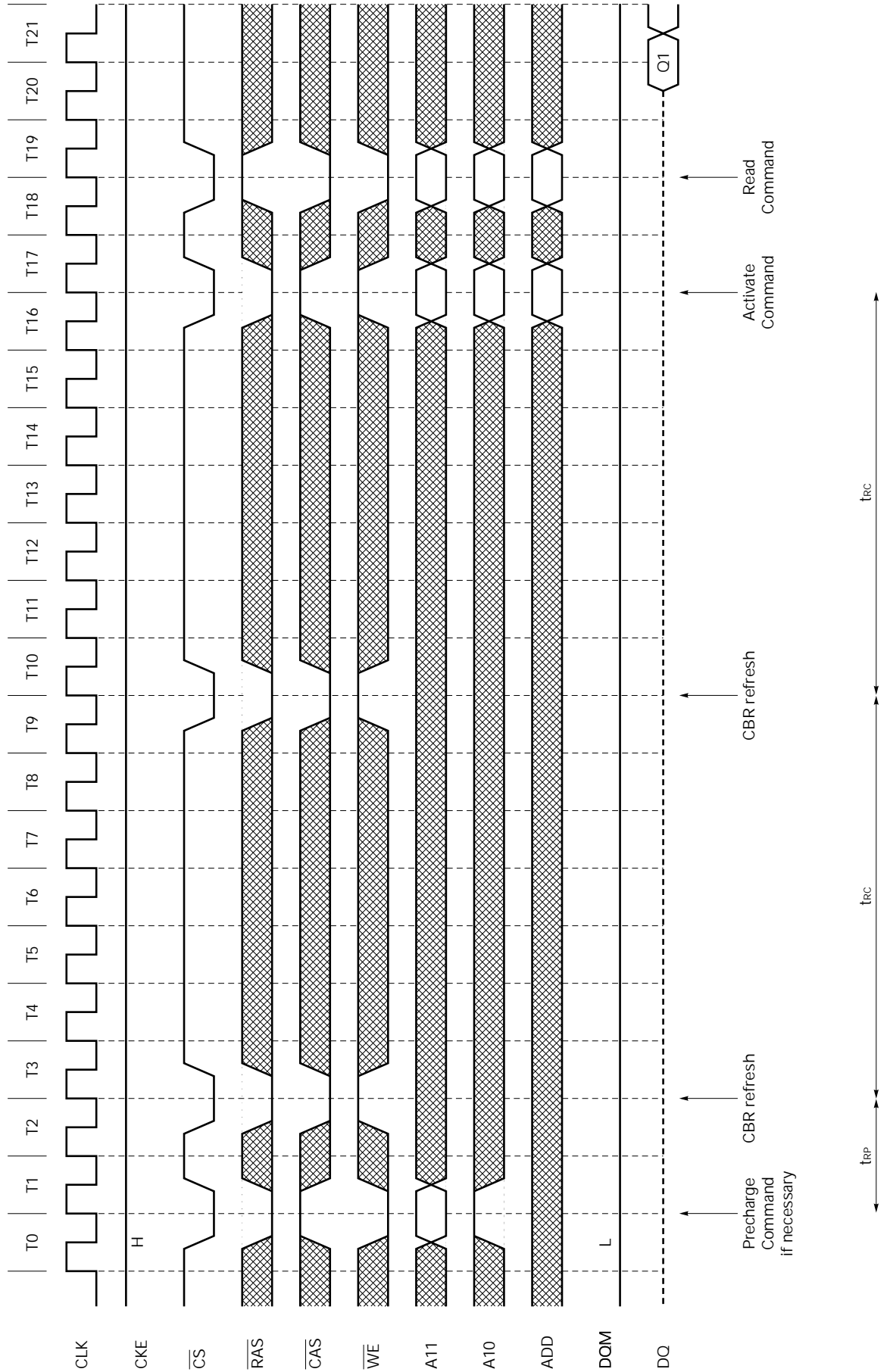


★ 12.9 Power Down Mode and Clock Mask

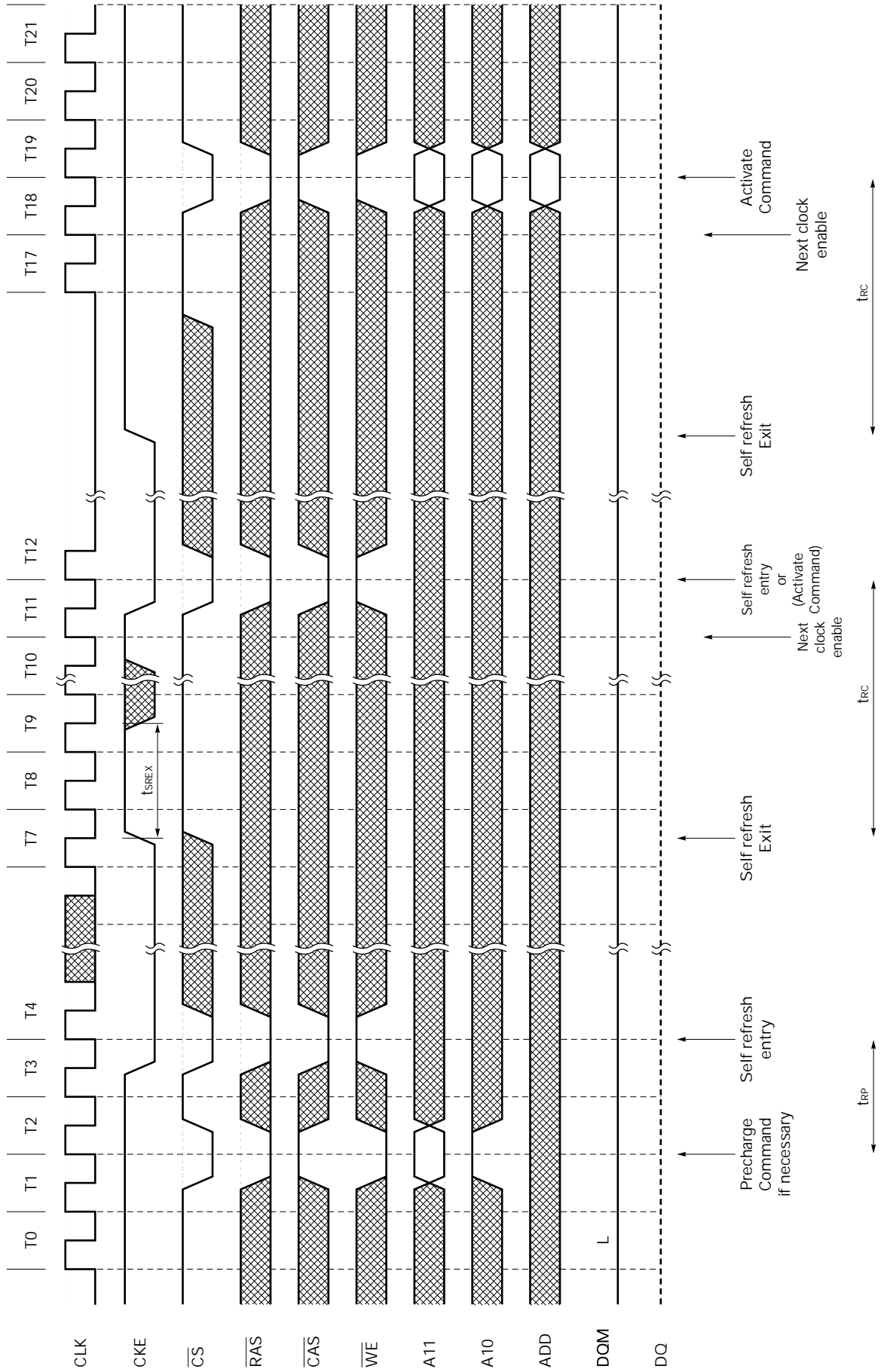
Burst length = 4 CAS latency = 2



12.10 CBR Refresh

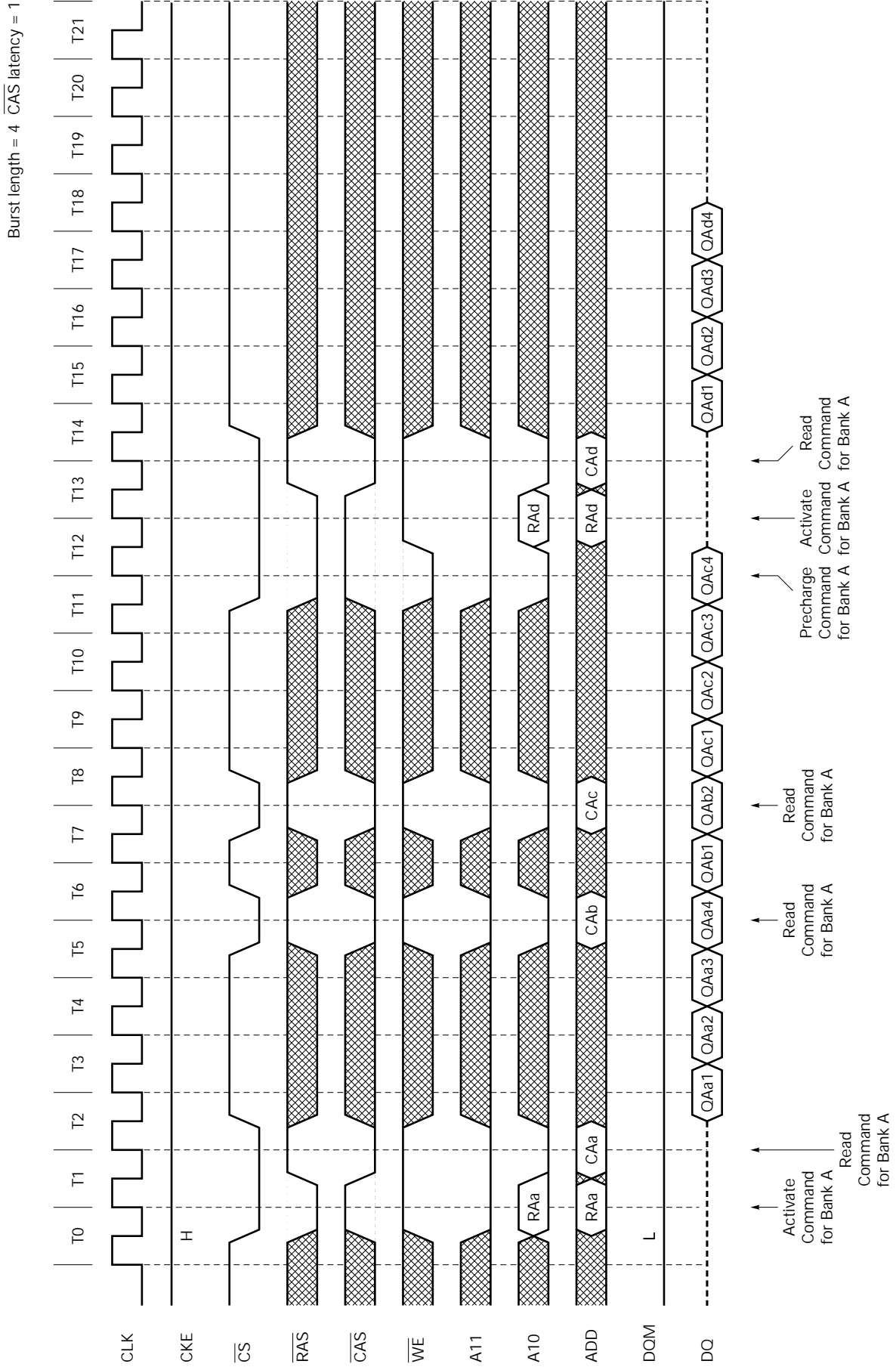


12.11 Self Refresh (entry and exit)



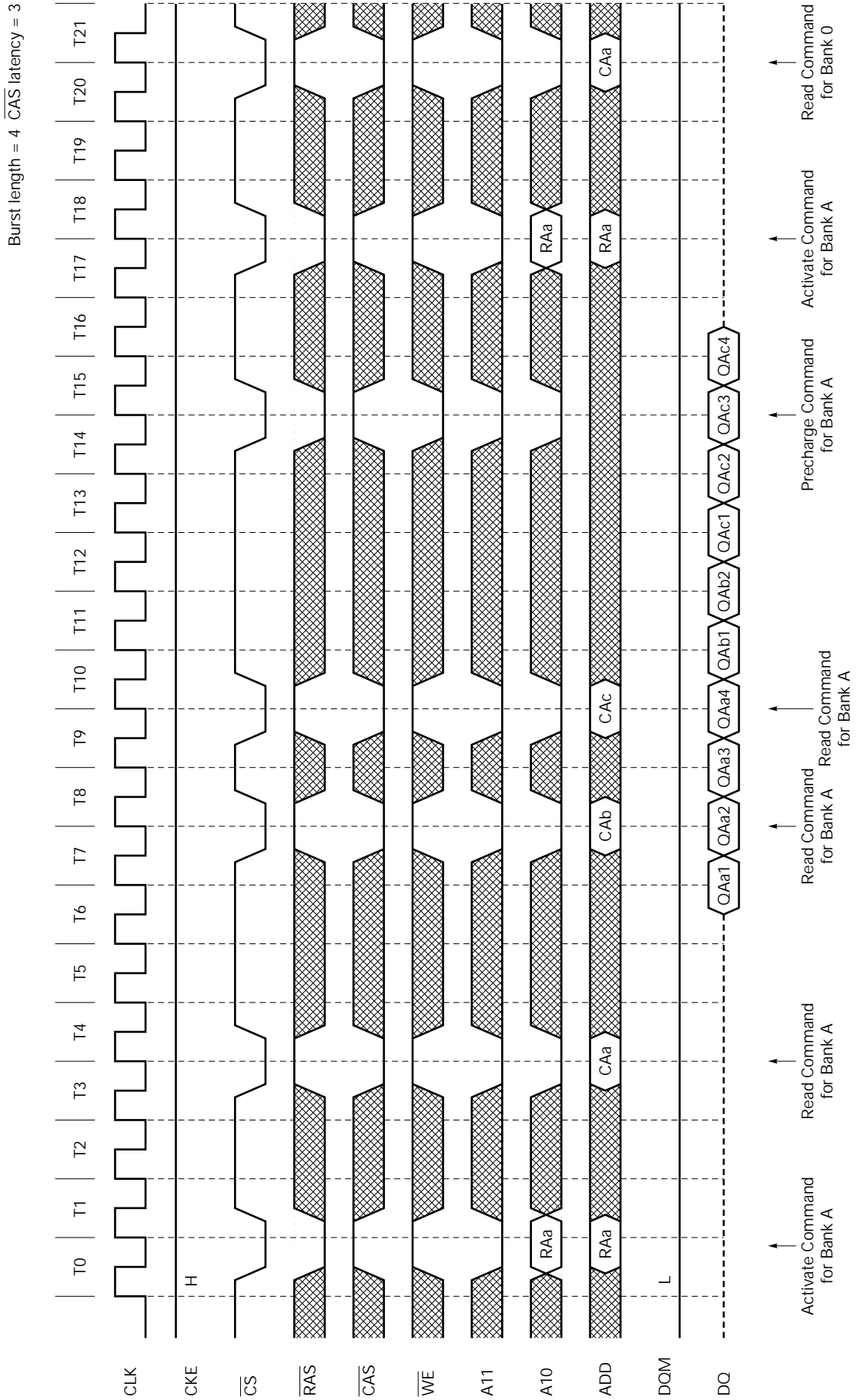


12.12 Random Column Read (Page with same bank) (1/3)



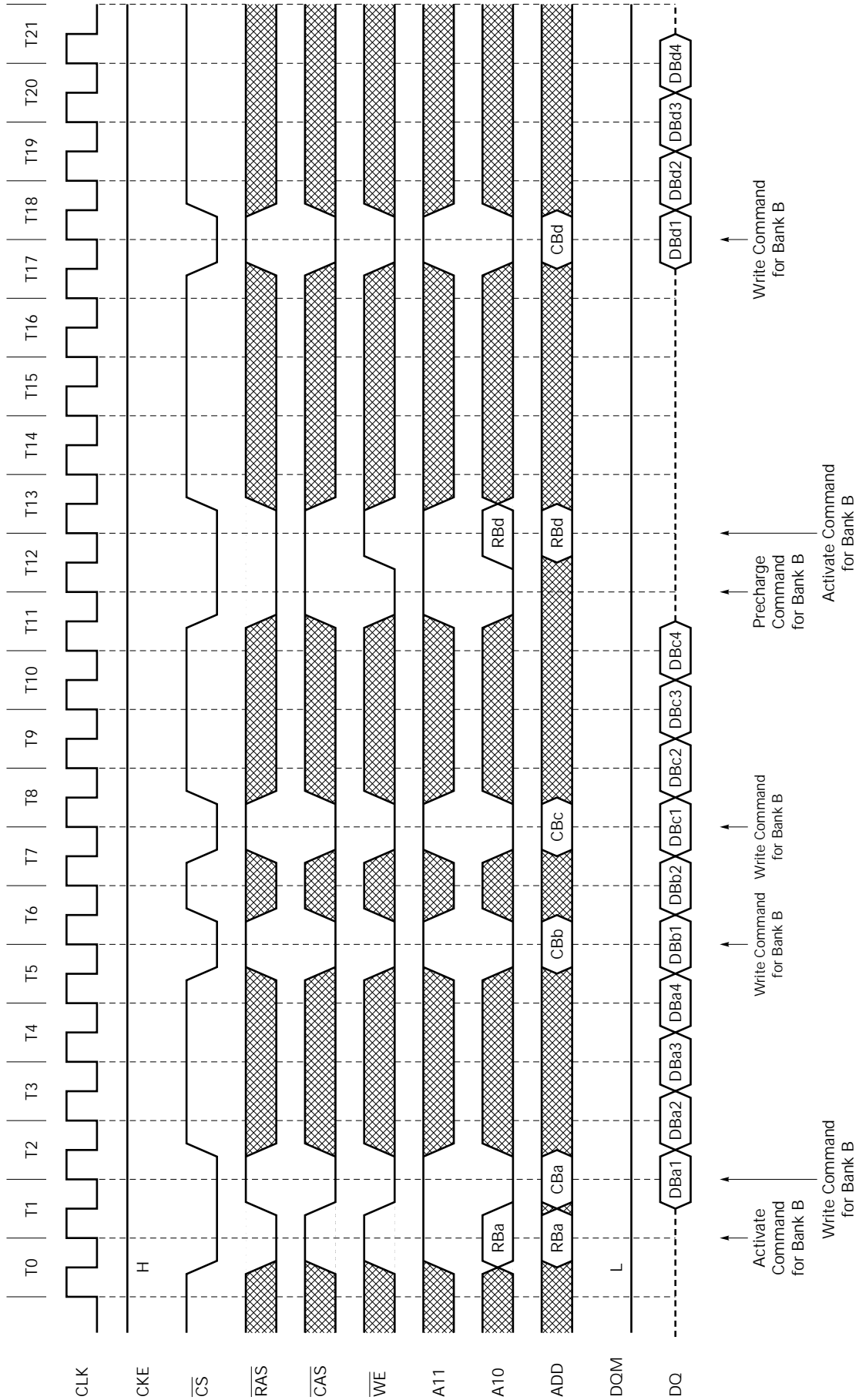


Random Column Read (Page with same bank) (3/3)



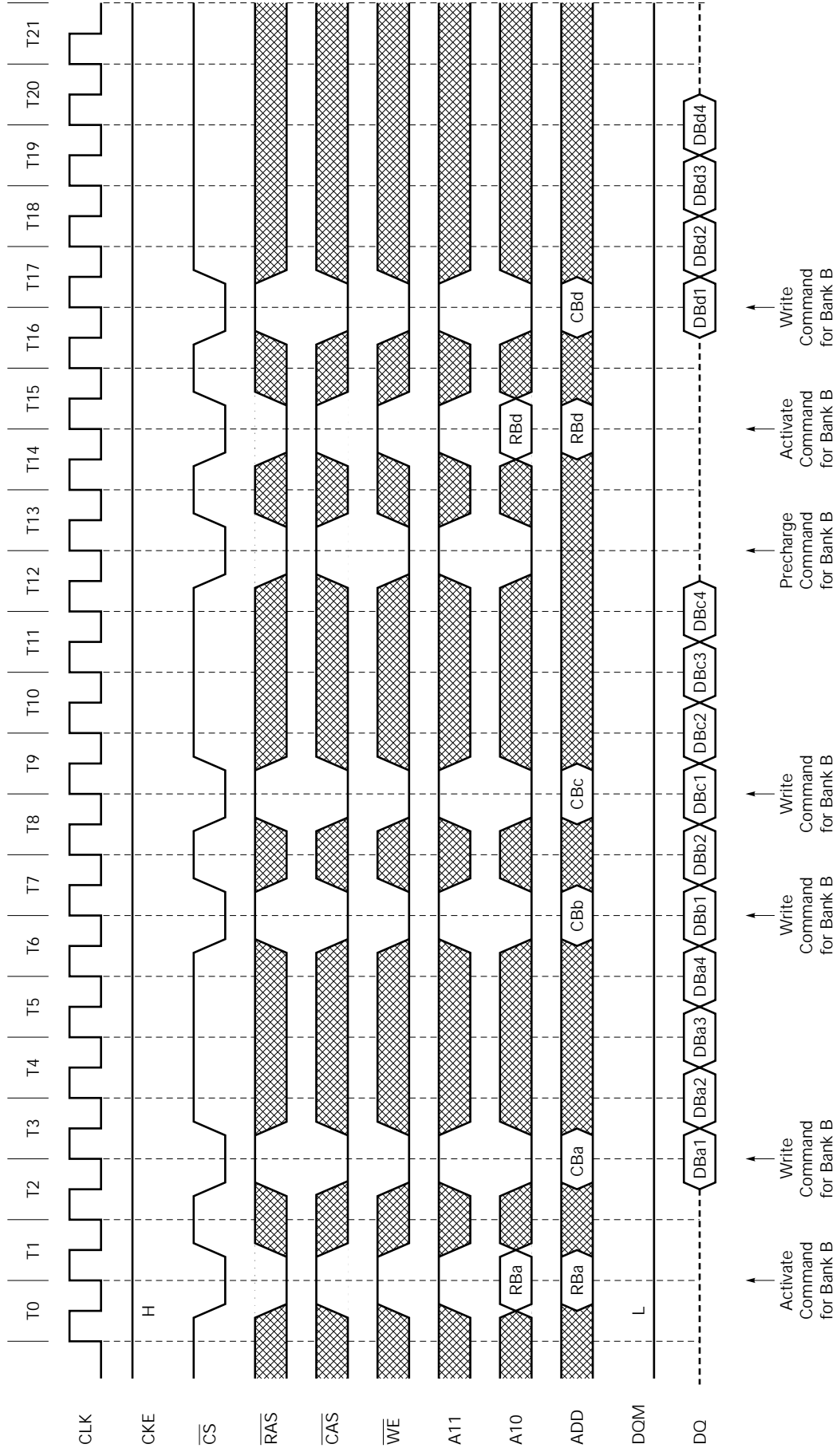
12.13 Random Column Write (Page with same bank) (1/3)

Burst length = 4 CAS latency = 1



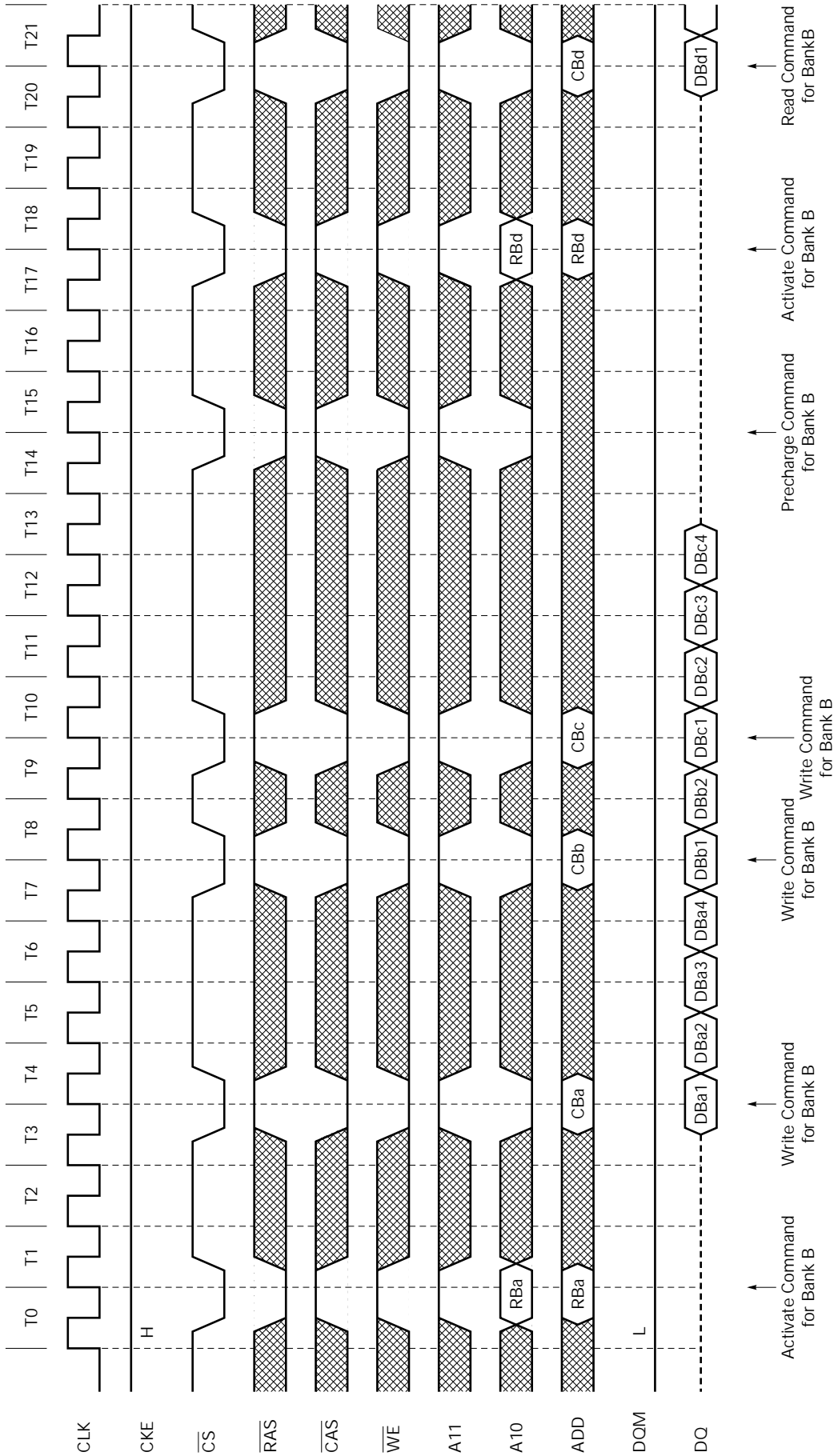
★ Random Column Write (Page with same bank) (2/3)

Burst length = 4 CAS latency = 2

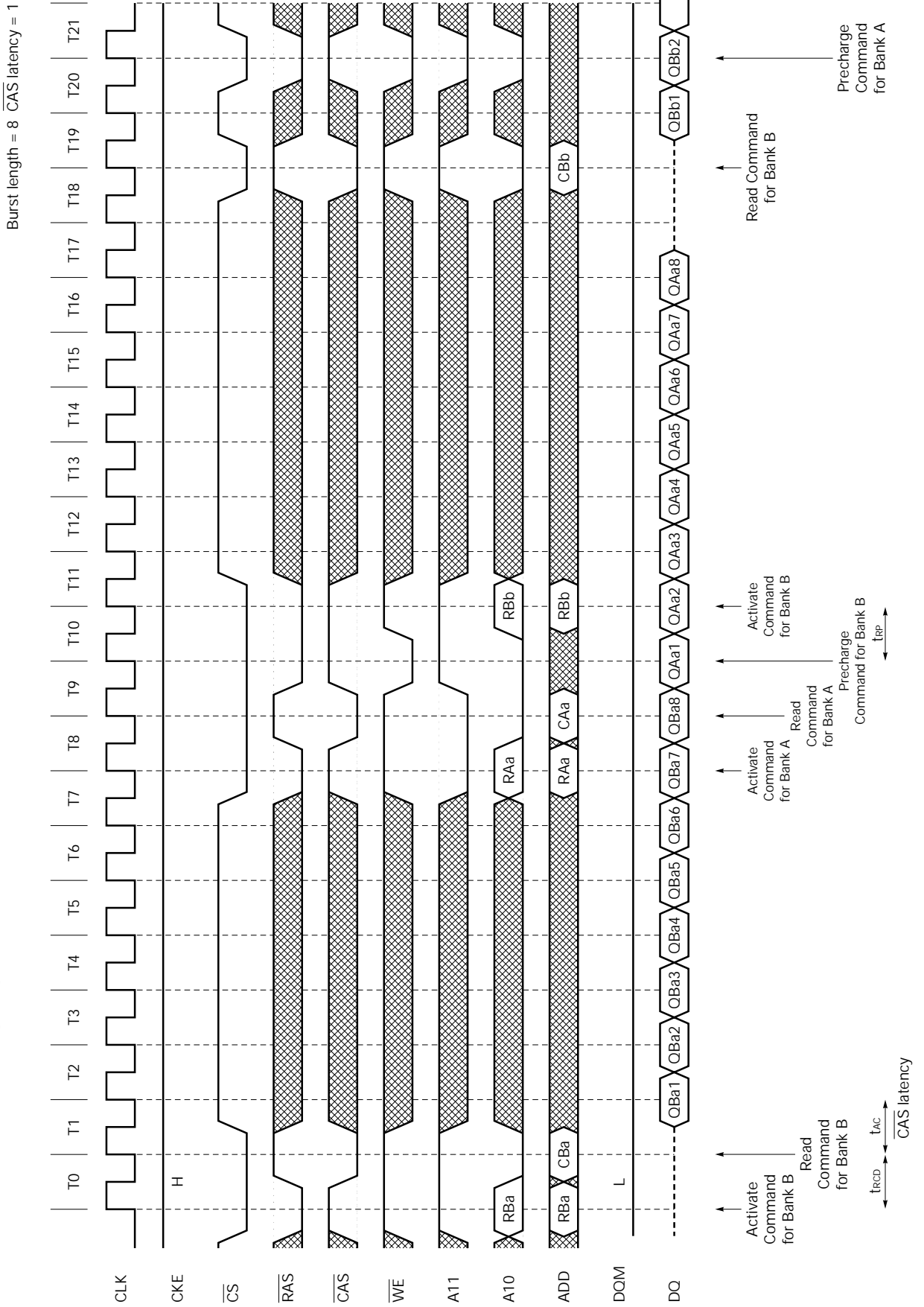


★ Random Column Write (Page with same bank) (3/3)

Burst length = 4 CAS latency = 3

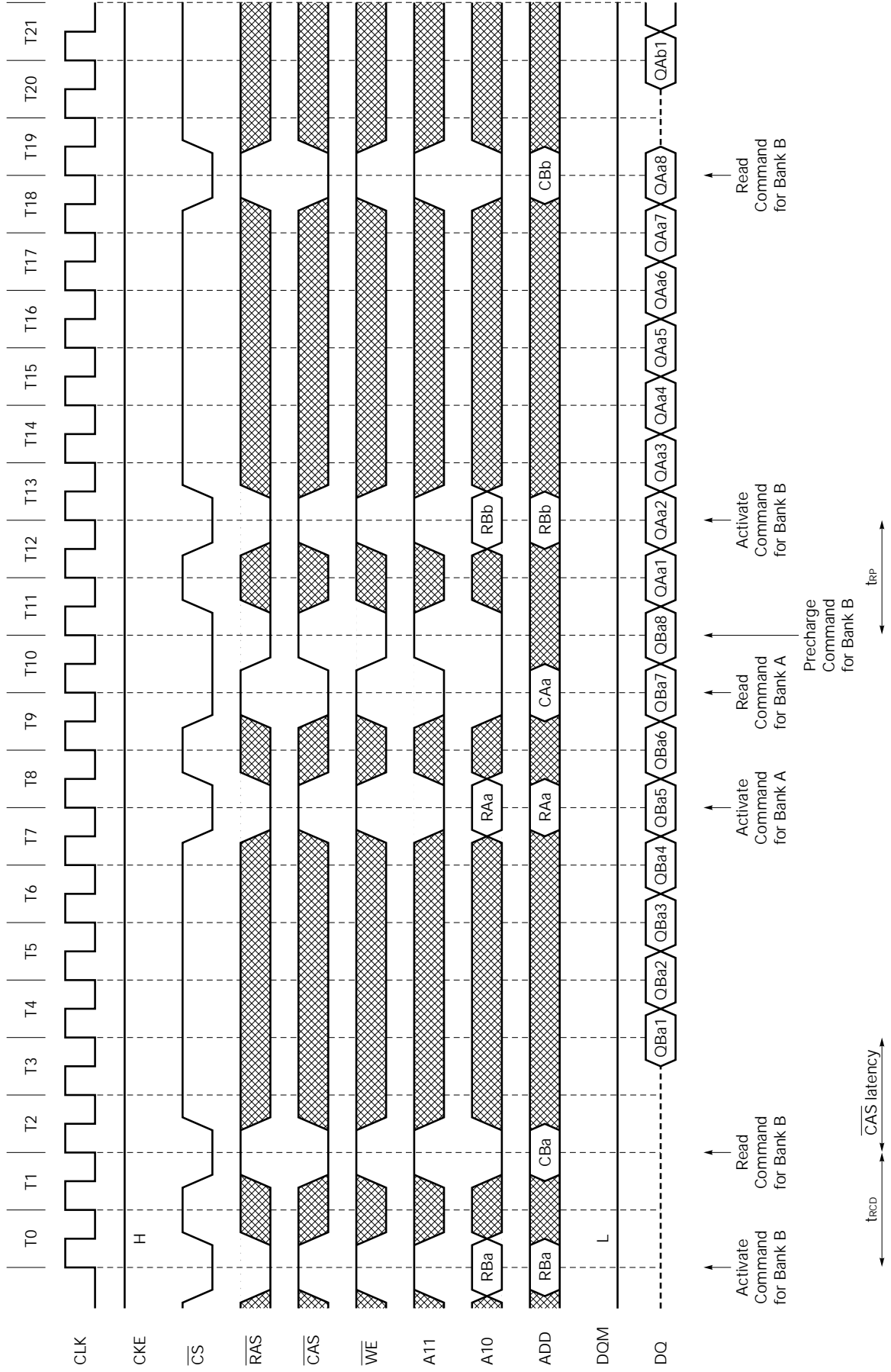


12.14 Random Row READ (Pingpong banks) (1/3)



Random Row READ (Pingpong banks) (2/3)

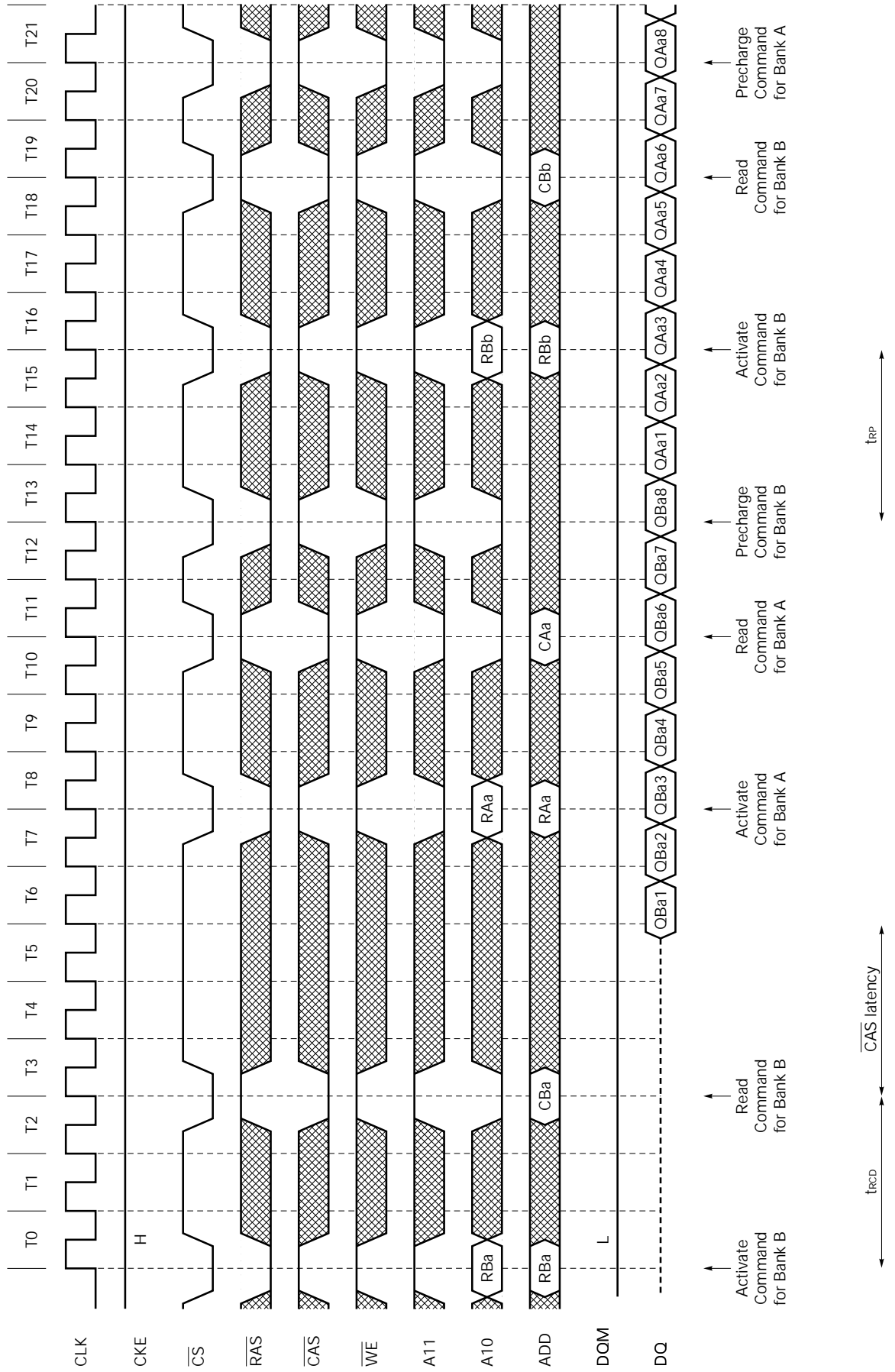
Burst length = 8 CAS latency = 2





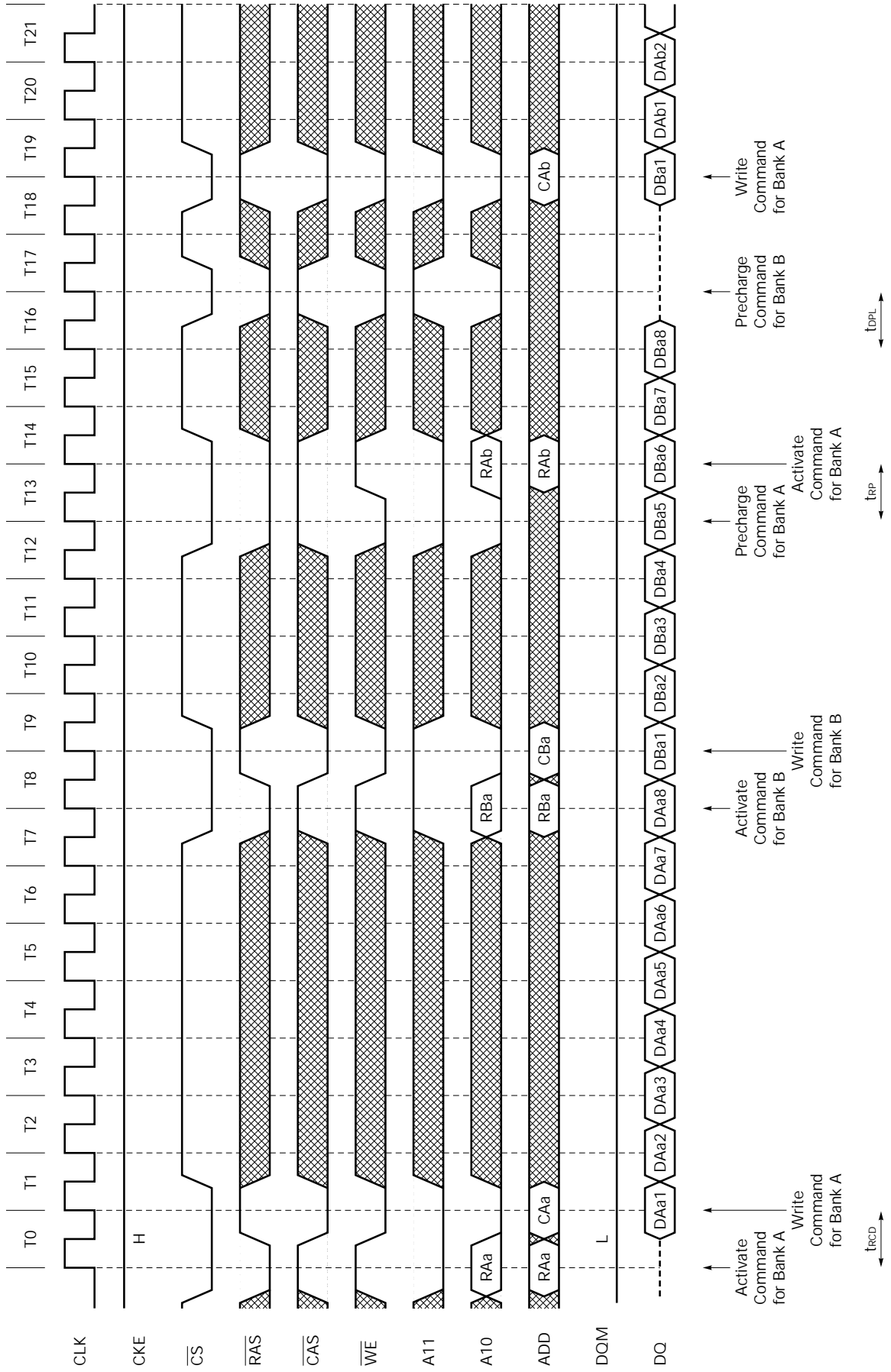
Random Row READ (Pingpong banks) (3/3)

Burst length = 8  $\overline{\text{CAS}}$  latency = 3



12.15 Random Row Write (Pingpong banks) (1/3)

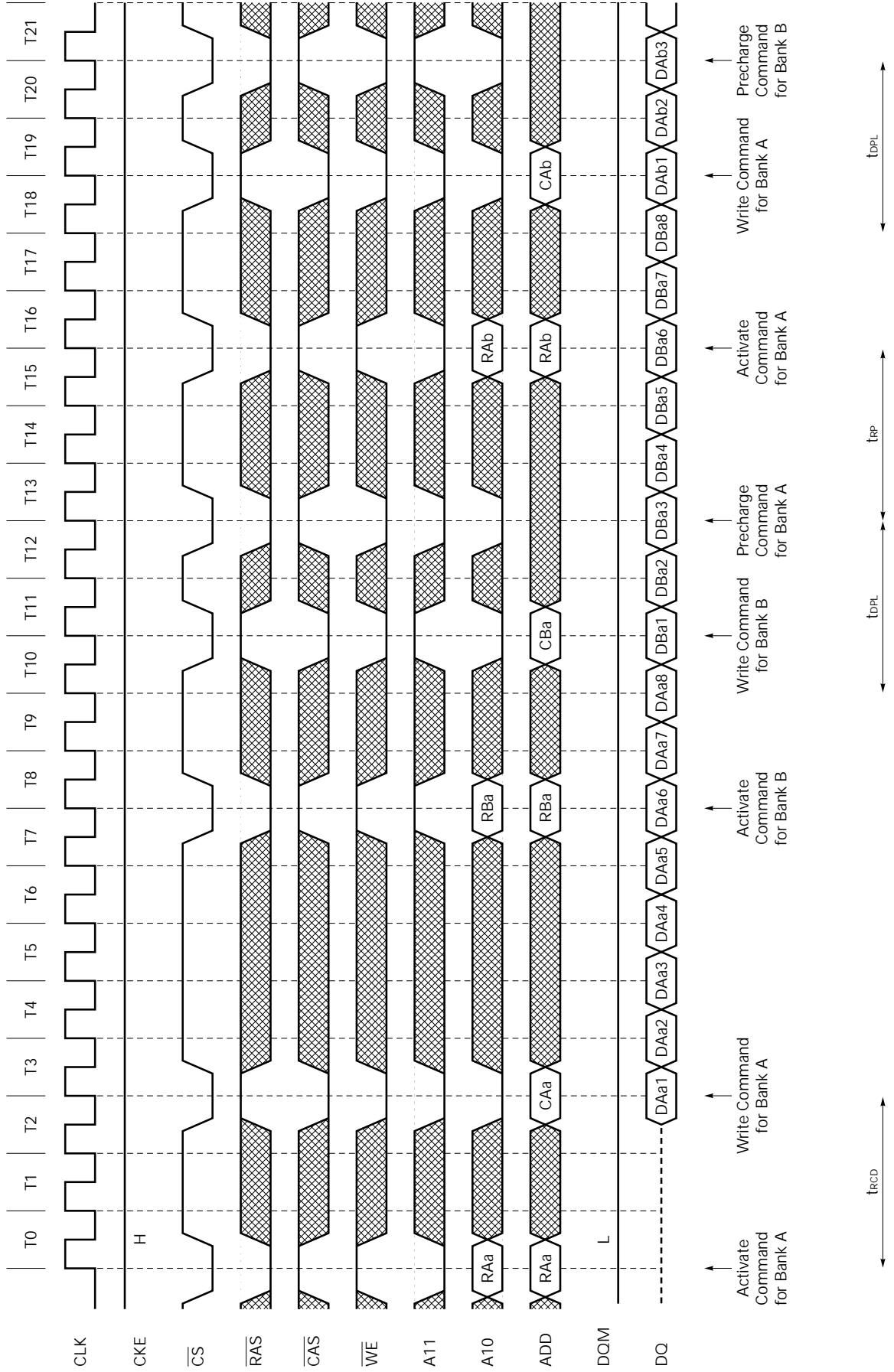
Burst length = 8  $\overline{\text{CAS}}$  latency = 1





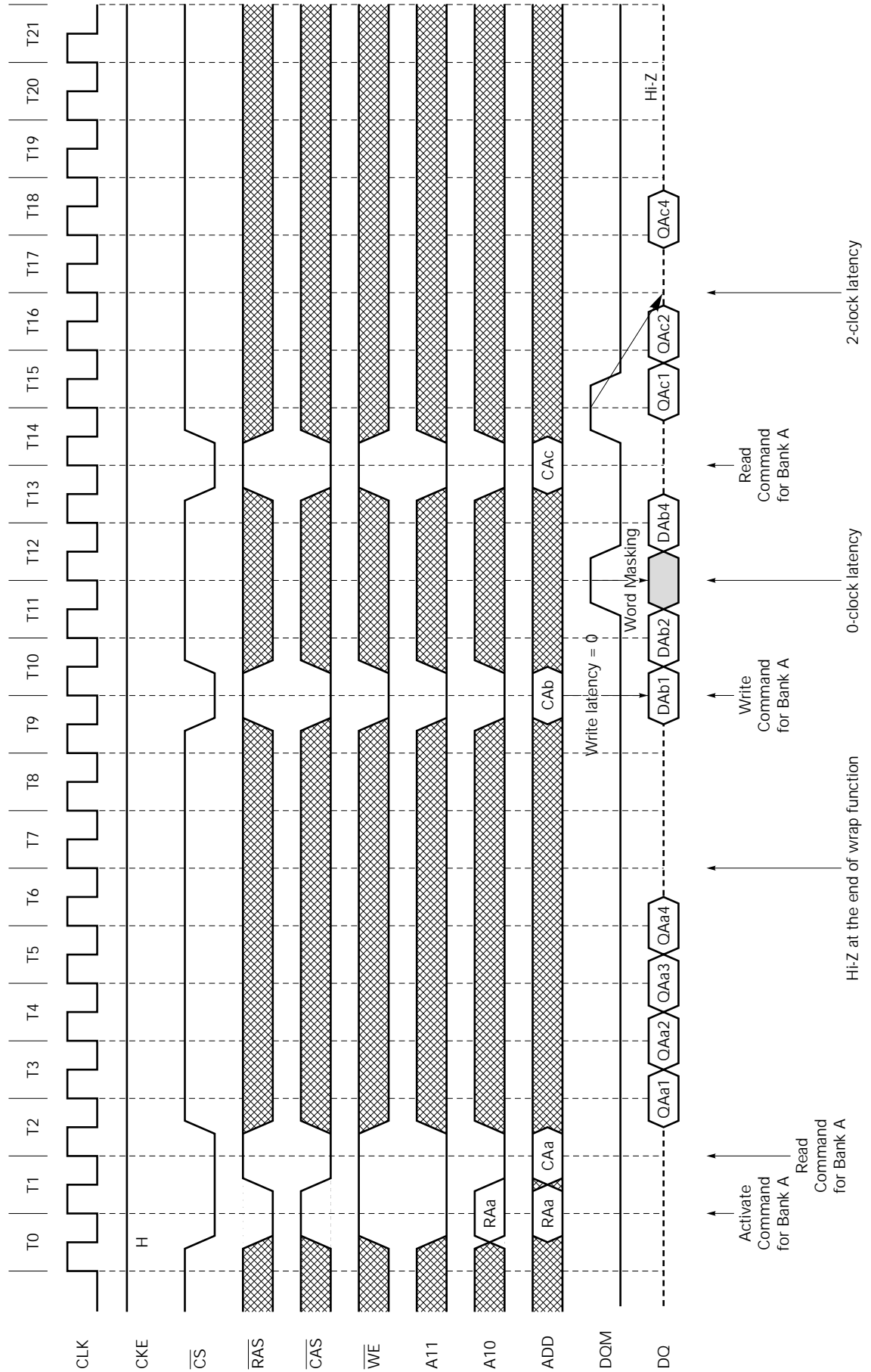
Random Row Write (Pingpong banks) (3/3)

Burst length = 8 CAS latency = 3



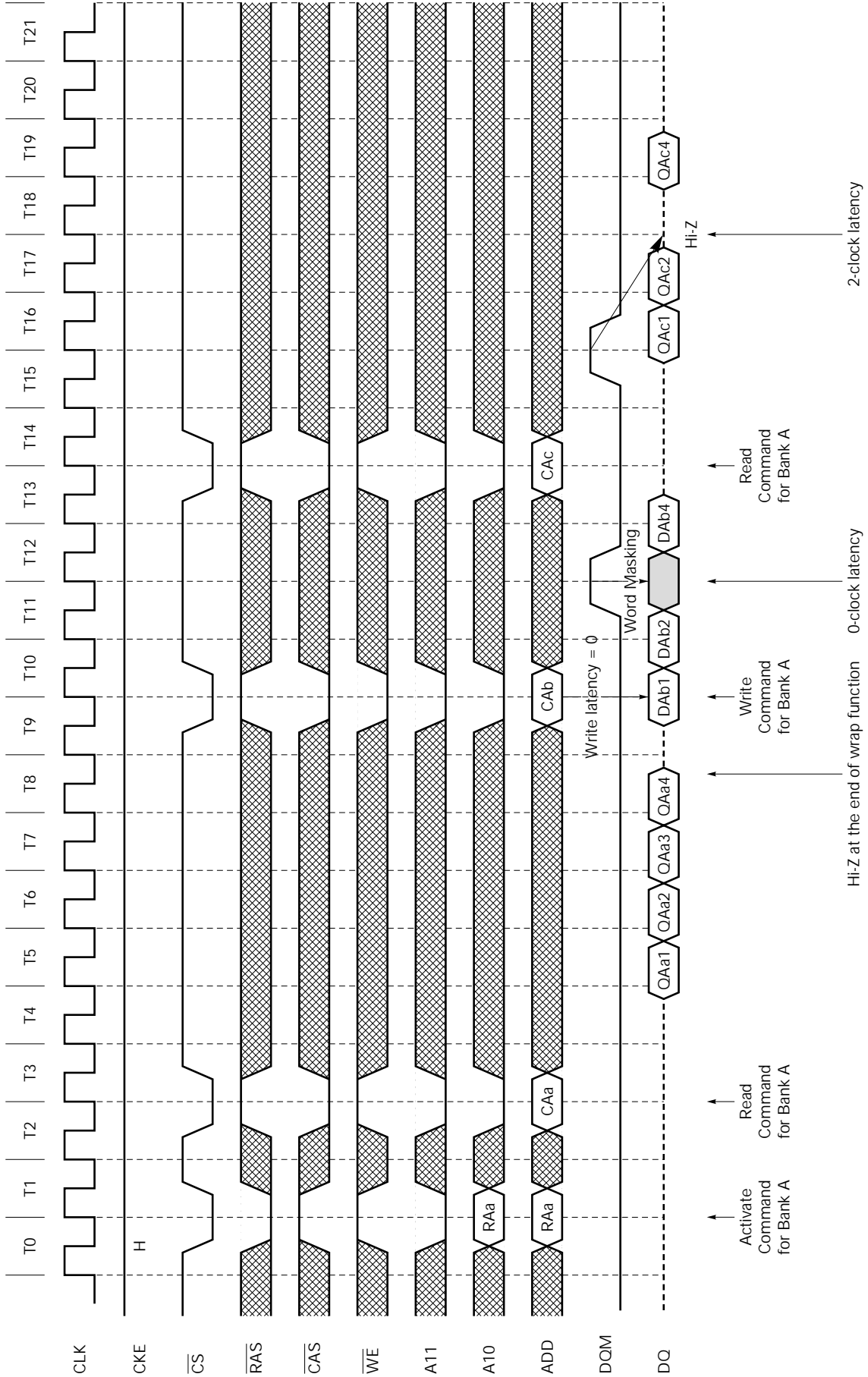
12.16 READ and WRITE (1/3)

Burst length = 4 CAS latency = 1



READ and WRITE (2/3)

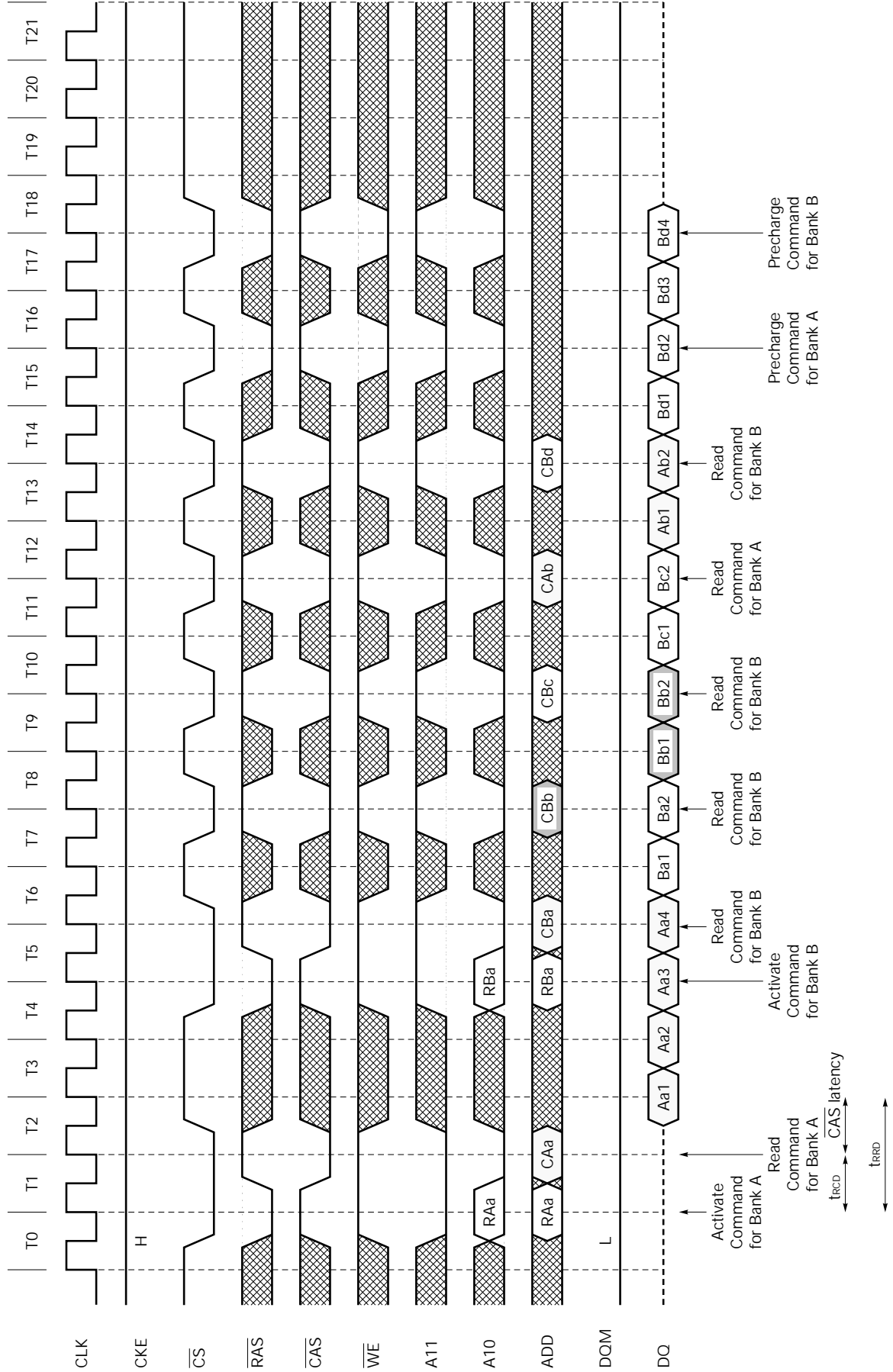
Burst length = 4 CAS latency = 2





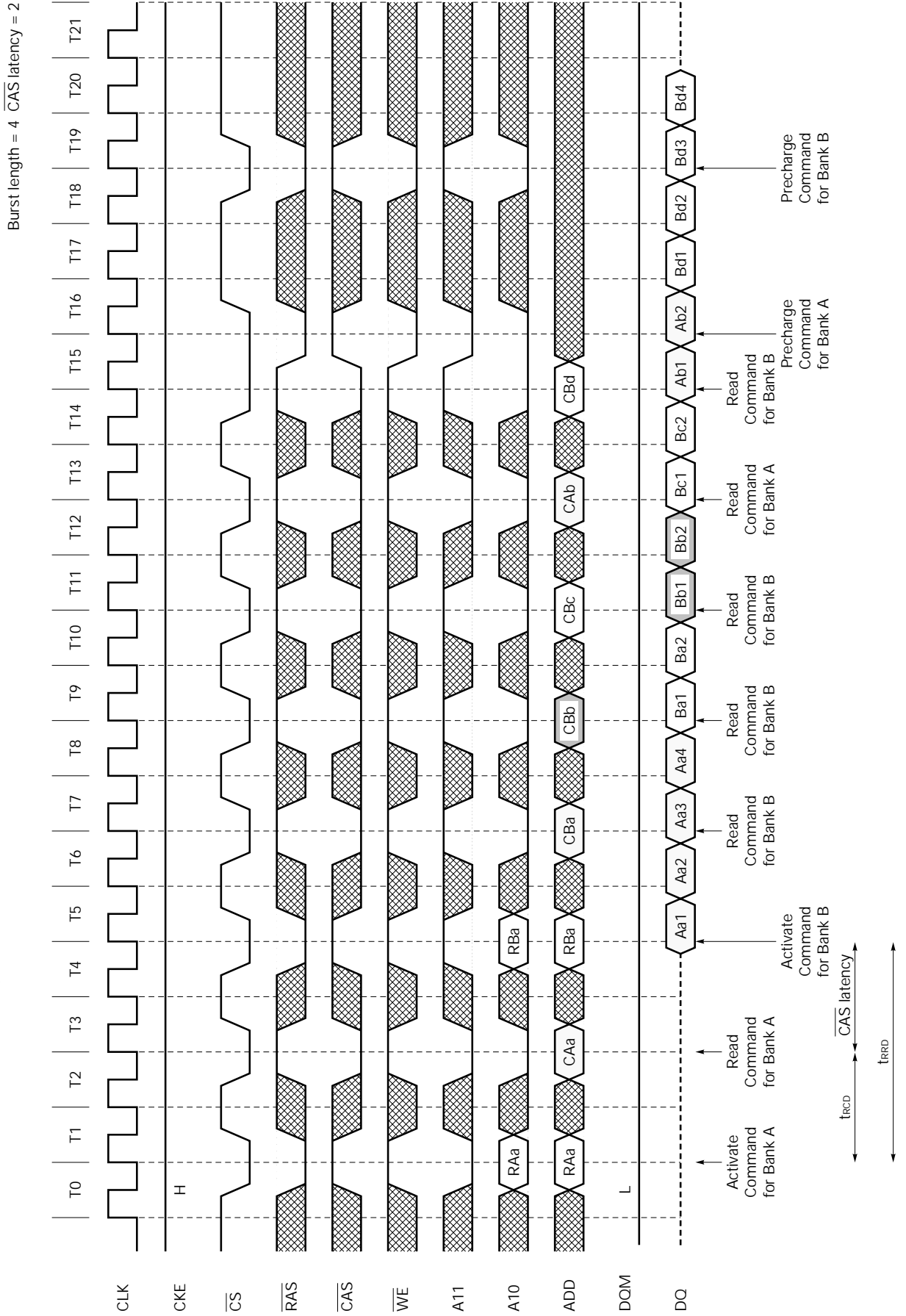
12.17 Interleaved Column READ Cycle (1/3)

Burst length = 4 CAS latency = 1



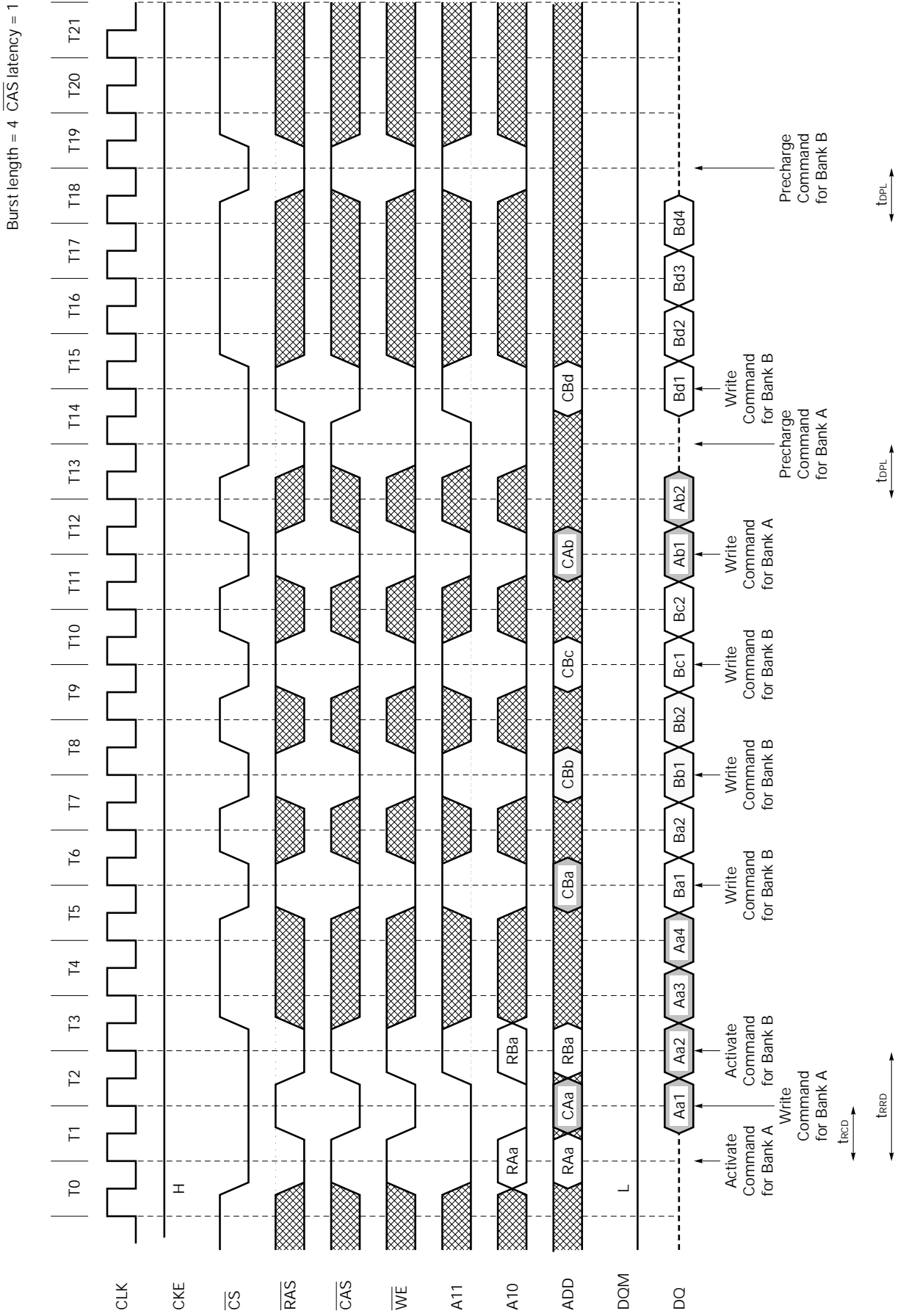


Interleaved Column READ Cycle (2/3)



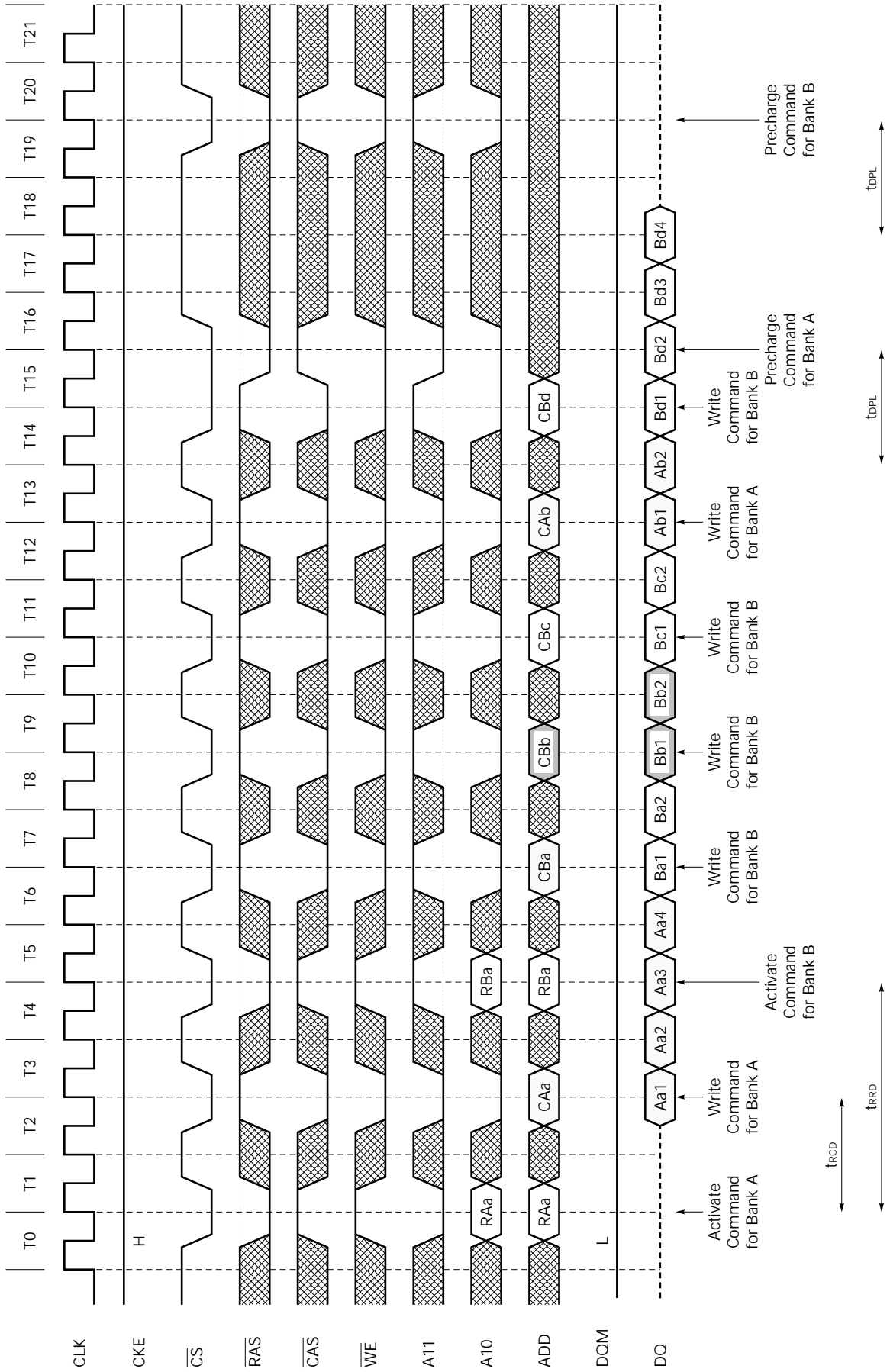


12.18 Interleaved Column WRITE Cycle (1/3)

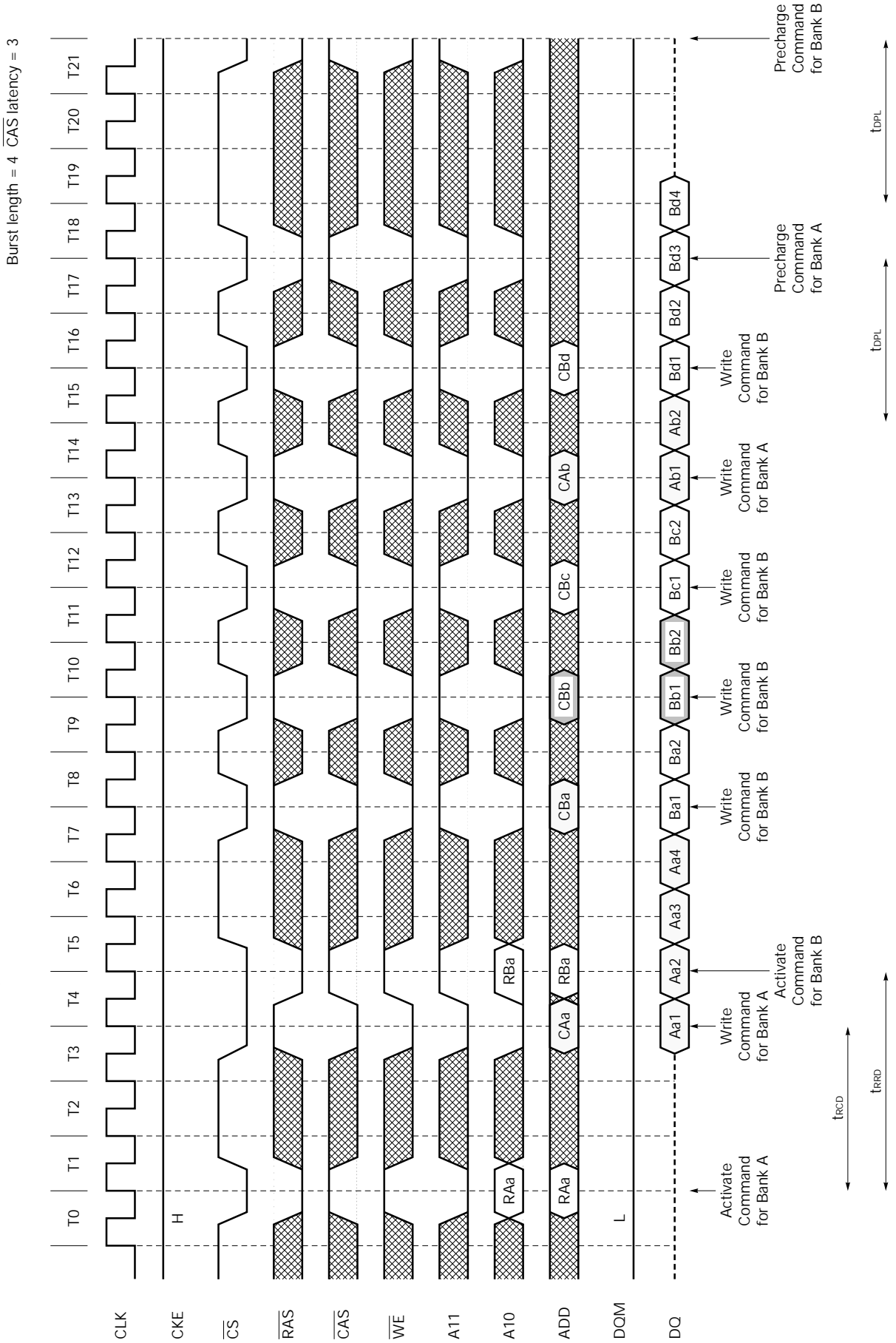


Interleaved Column WRITE Cycle (2/3)

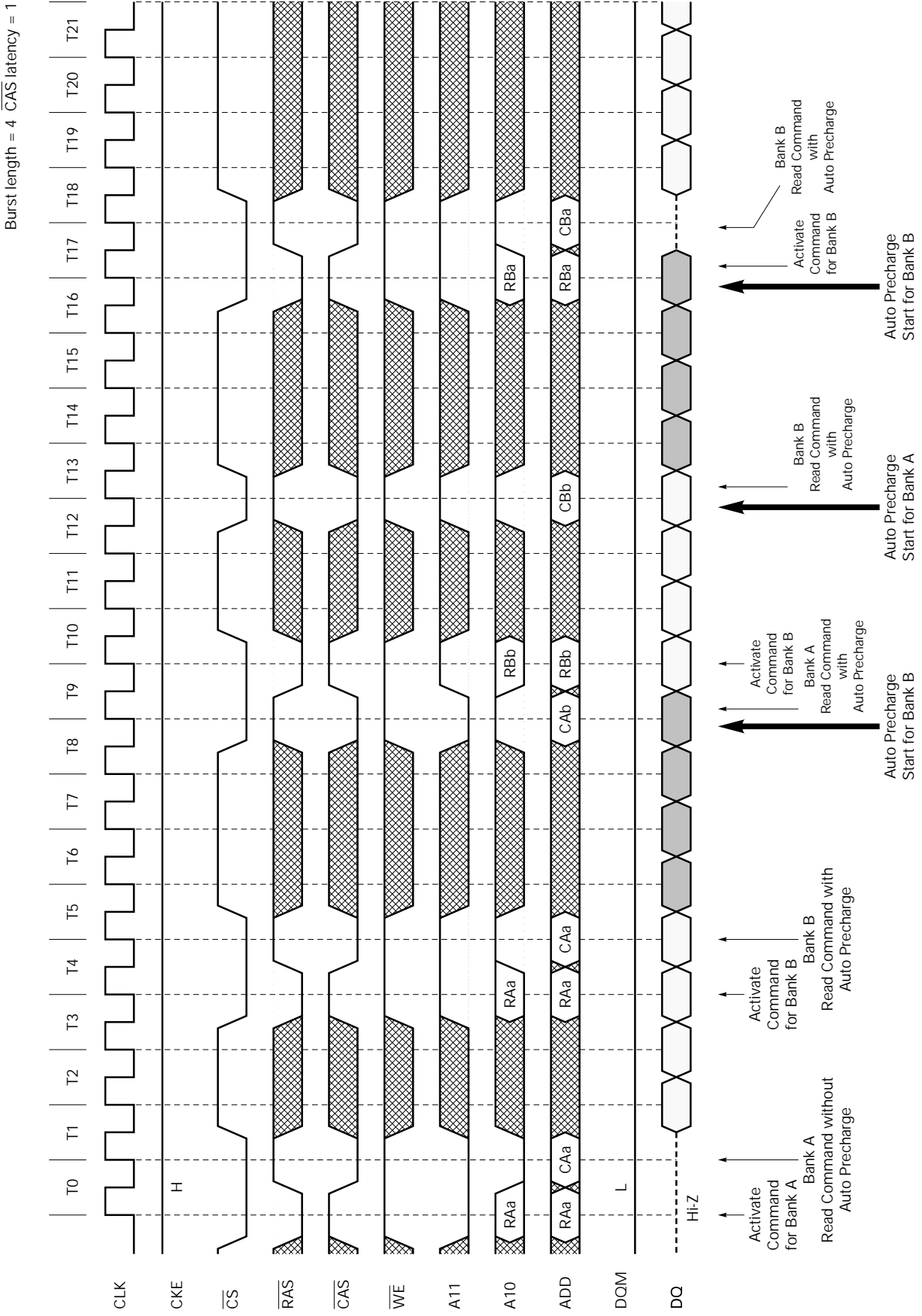
Burst length = 4 CAS latency = 2



Interleaved Column WRITE Cycle (3/3)

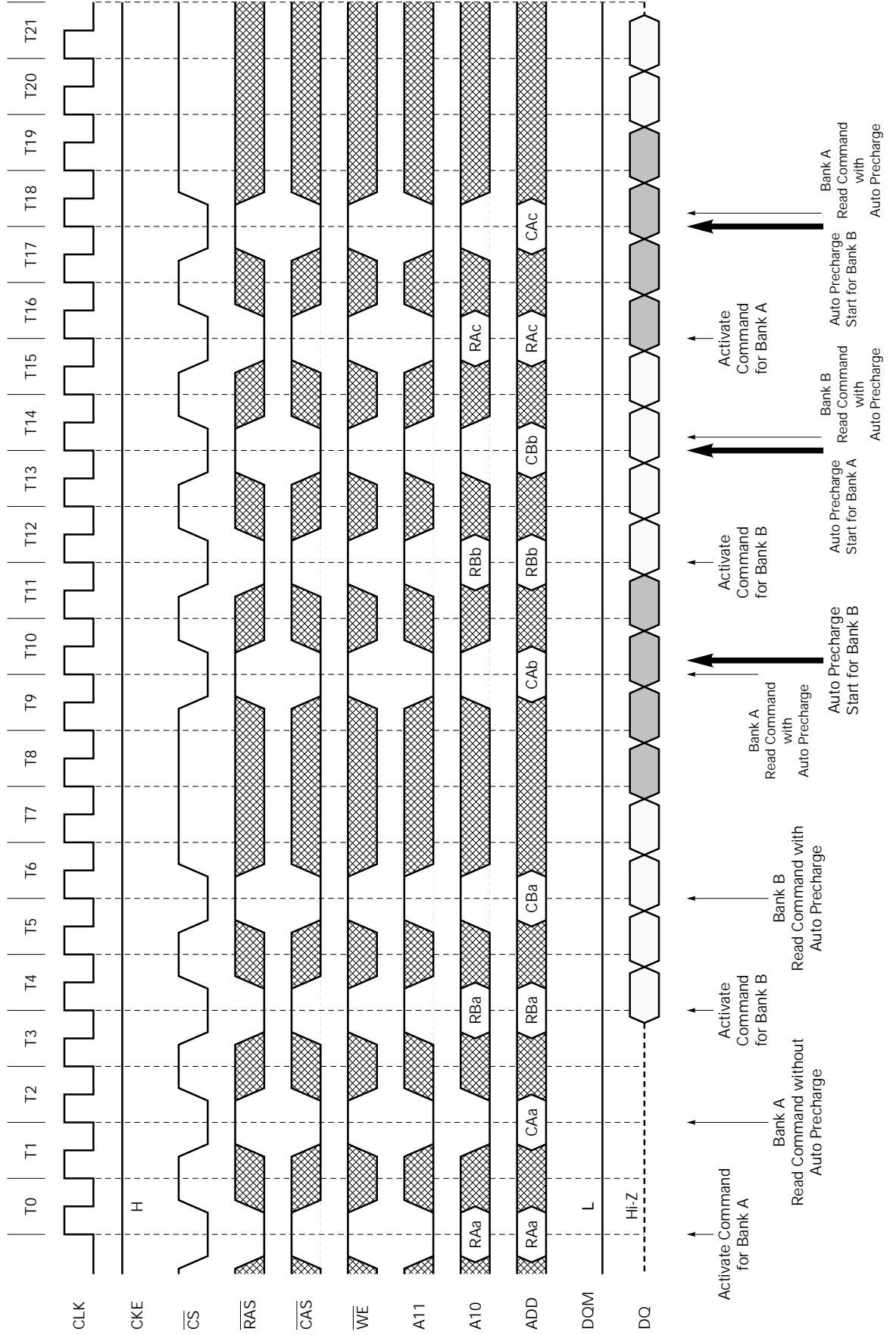


12.19 Auto Precharge after Read Burst (1/3)



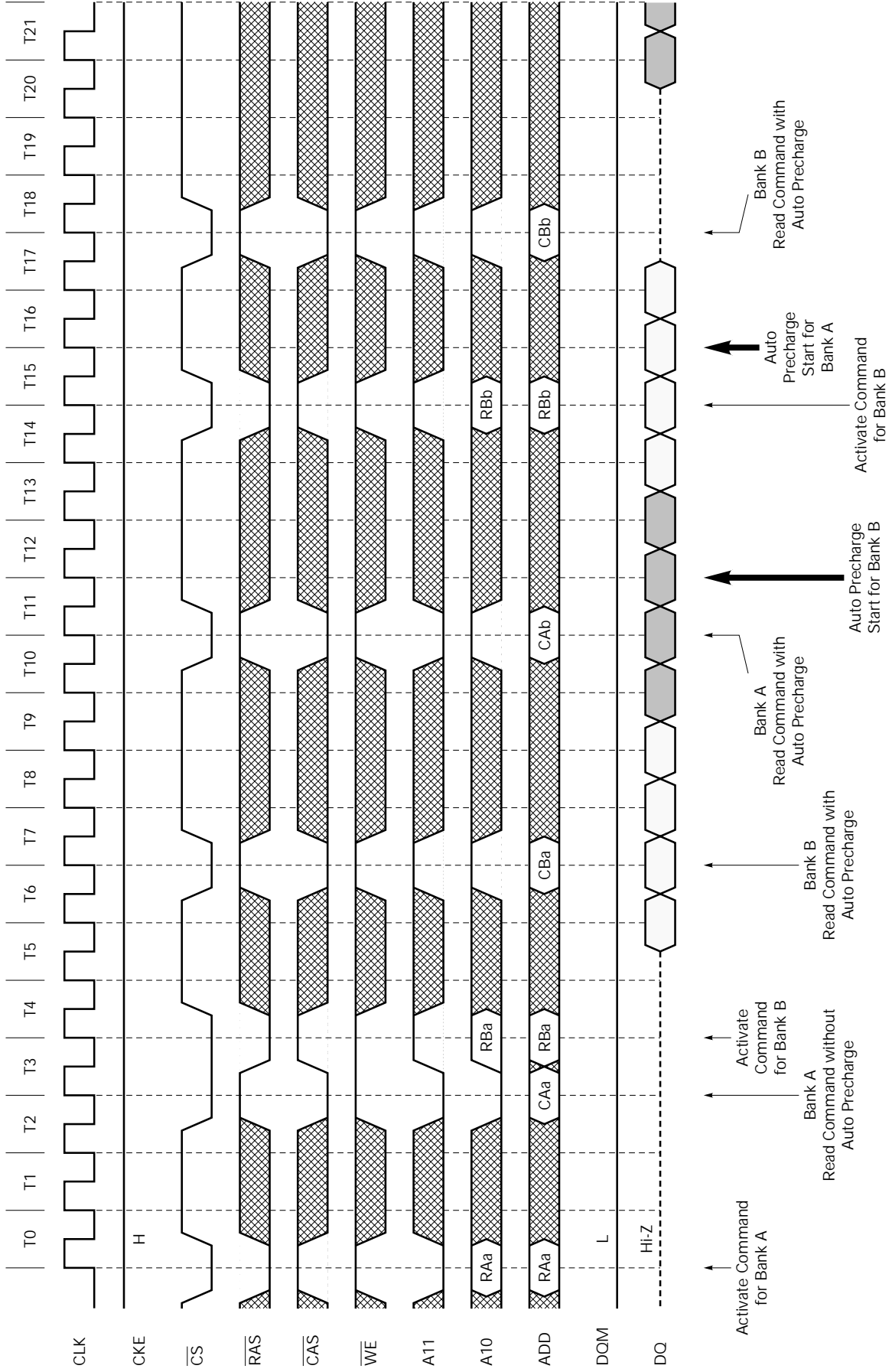
Auto Precharge after Read Burst (2/3)

Burst length = 4 CAS latency = 2



Auto Precharge after Read Burst (3/3)

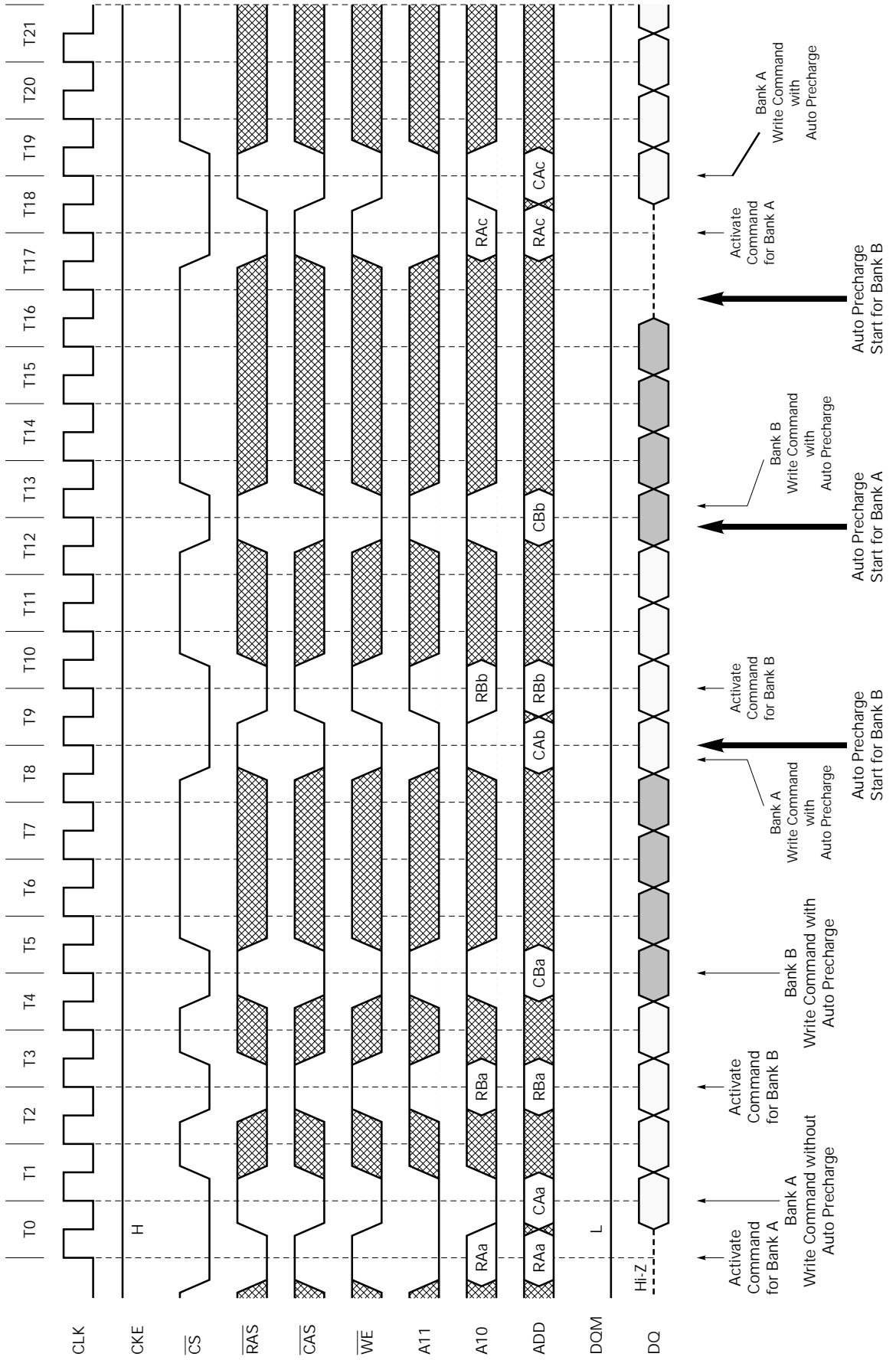
Burst length = 4 CAS latency = 3





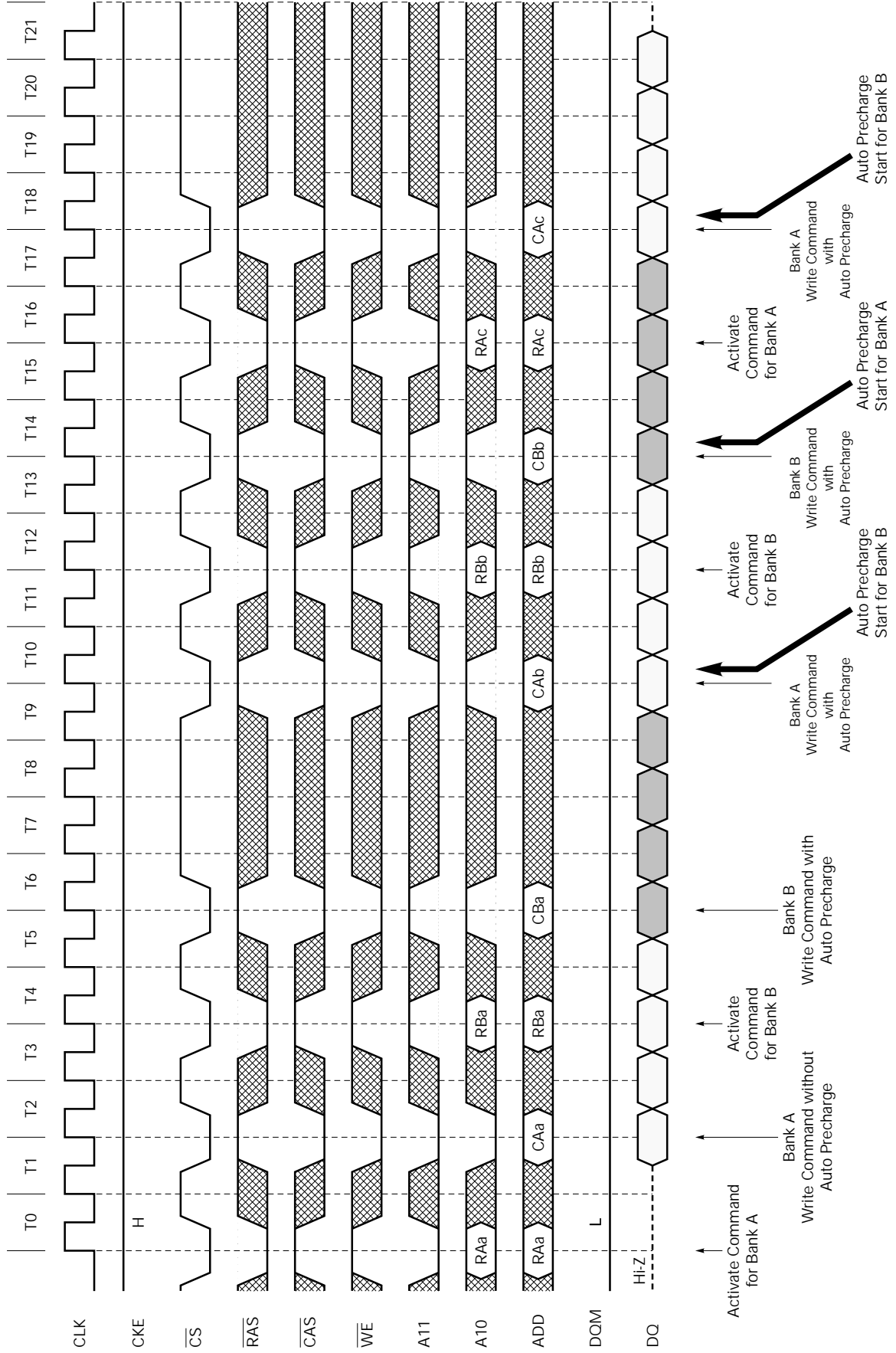
12.20 Auto Precharge after Write Burst (1/3)

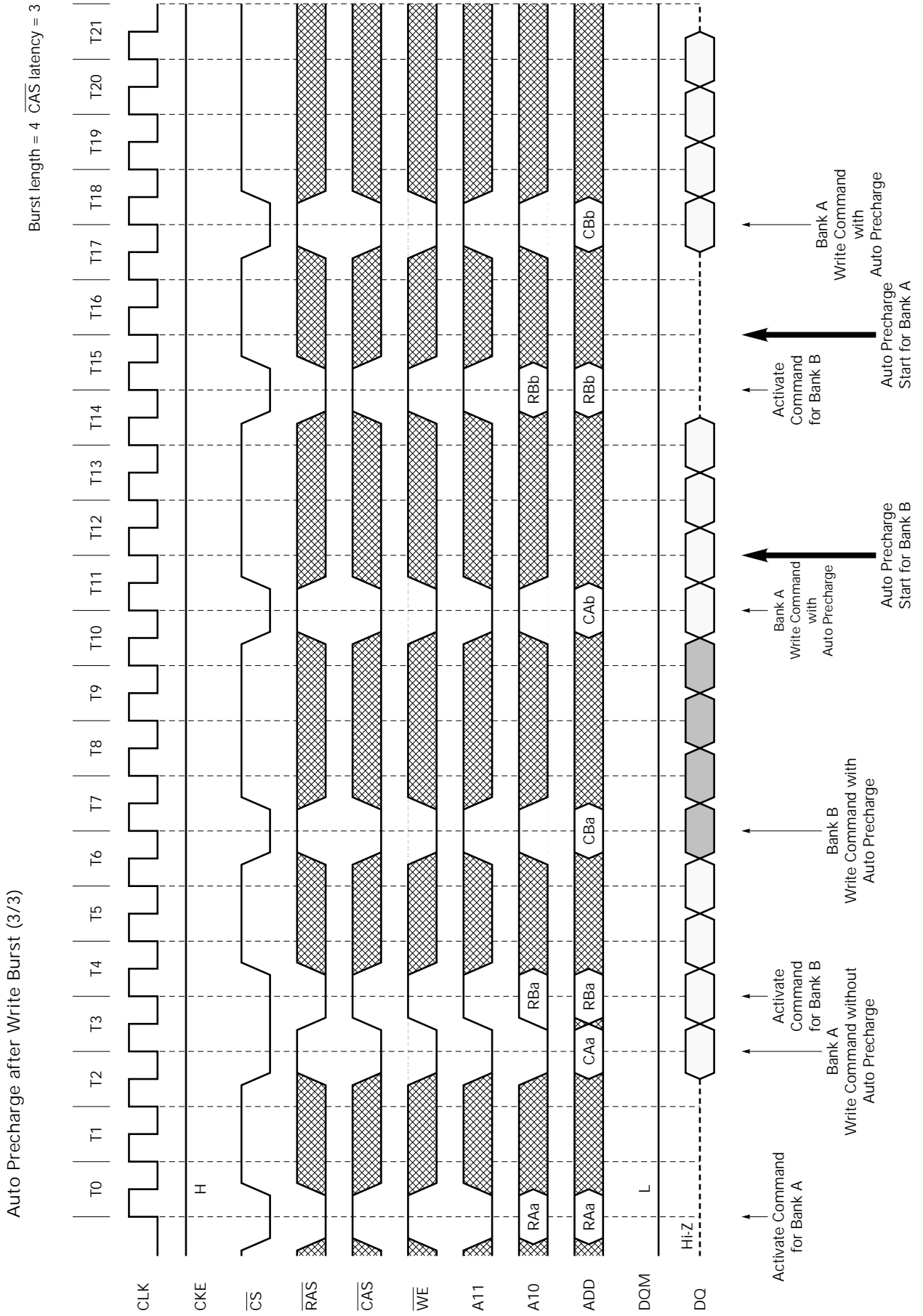
Burst length = 4  $\overline{\text{CAS}}$  latency = 1



Auto Precharge after Write Burst (2/3)

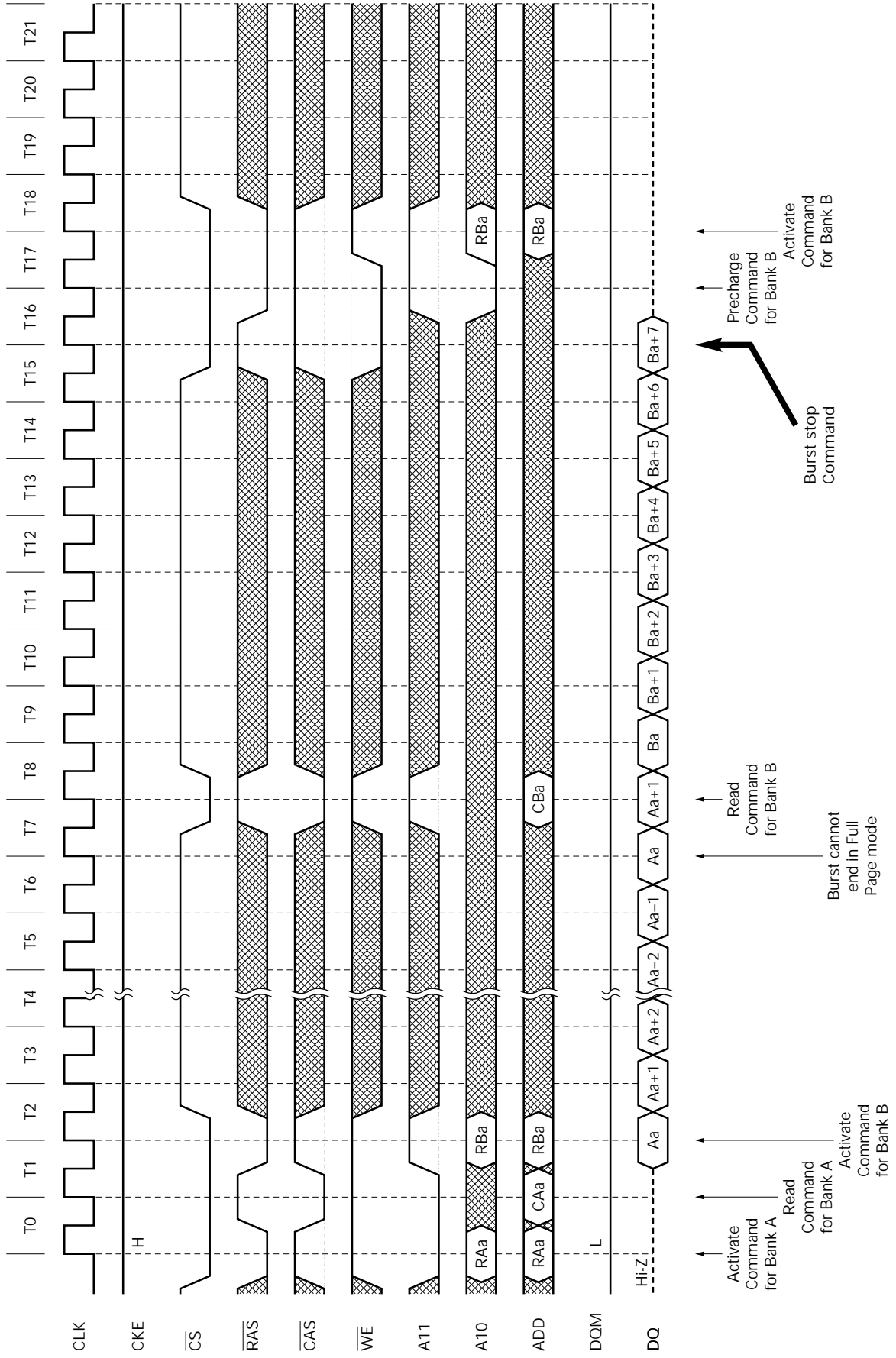
Burst length = 4 CAS latency = 2





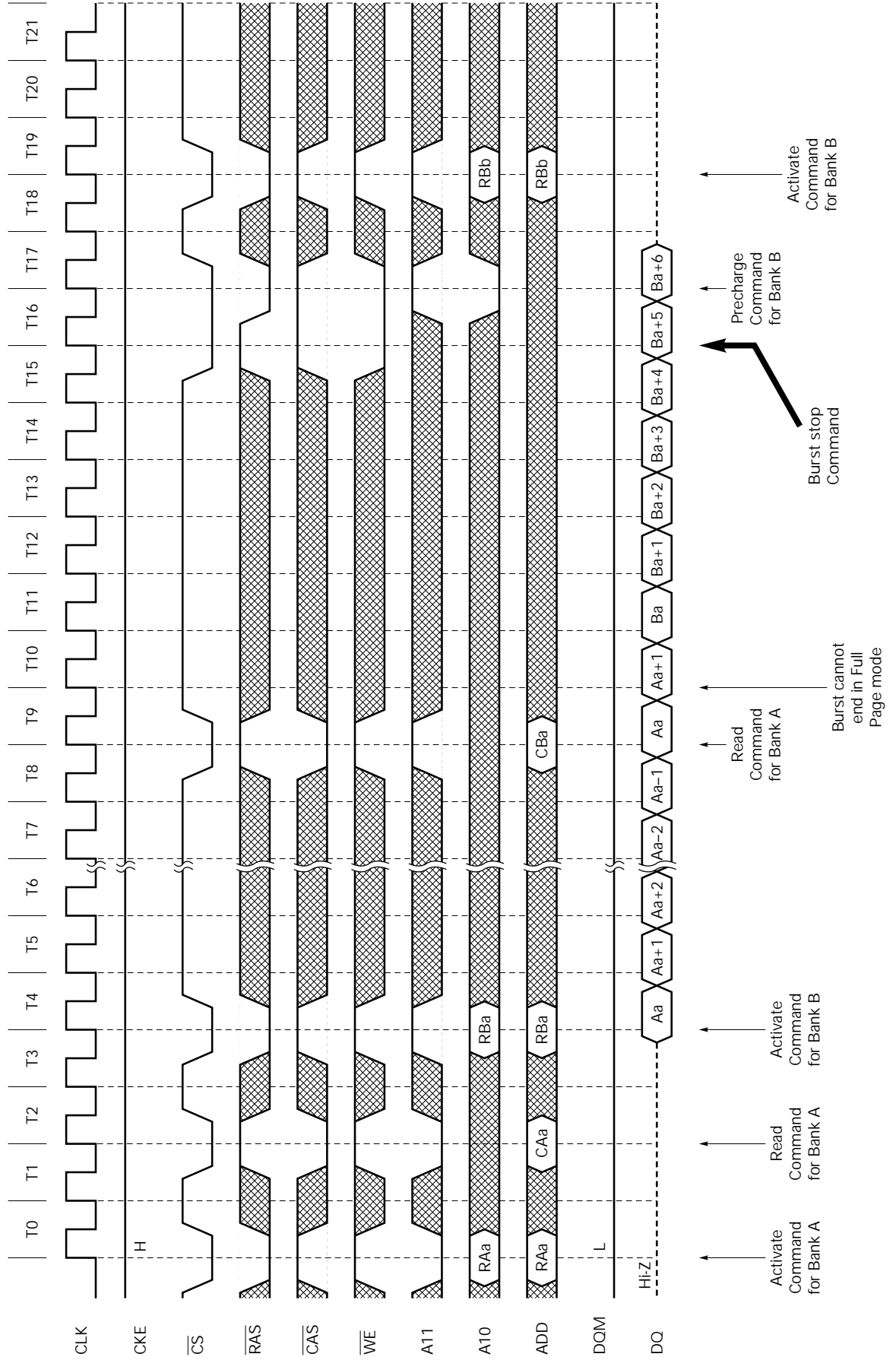
12.21 Full Page READ Cycle (1/3)

CAS latency = 1



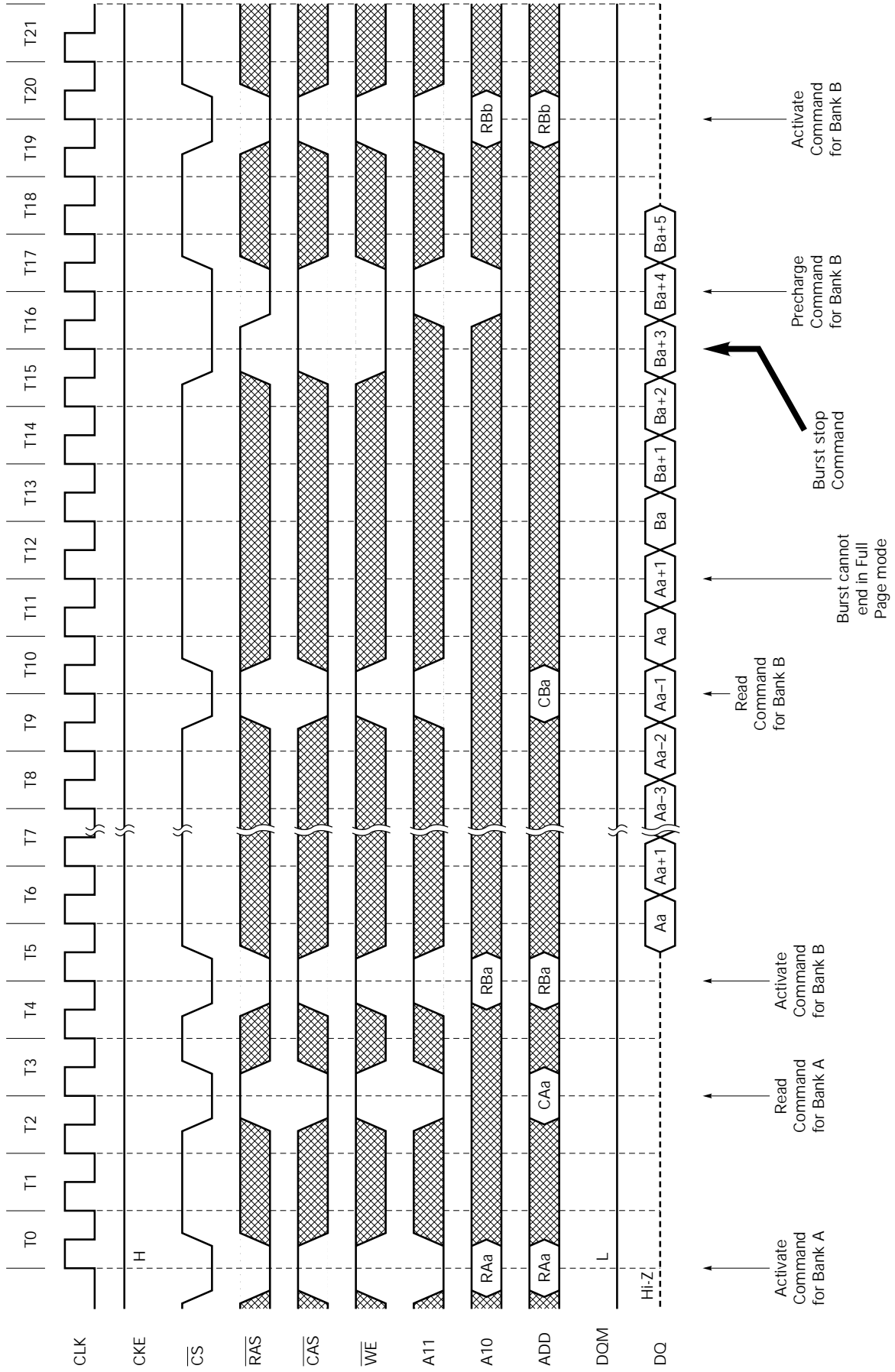
Full Page READ Cycle (2/3)

CAS latency = 2

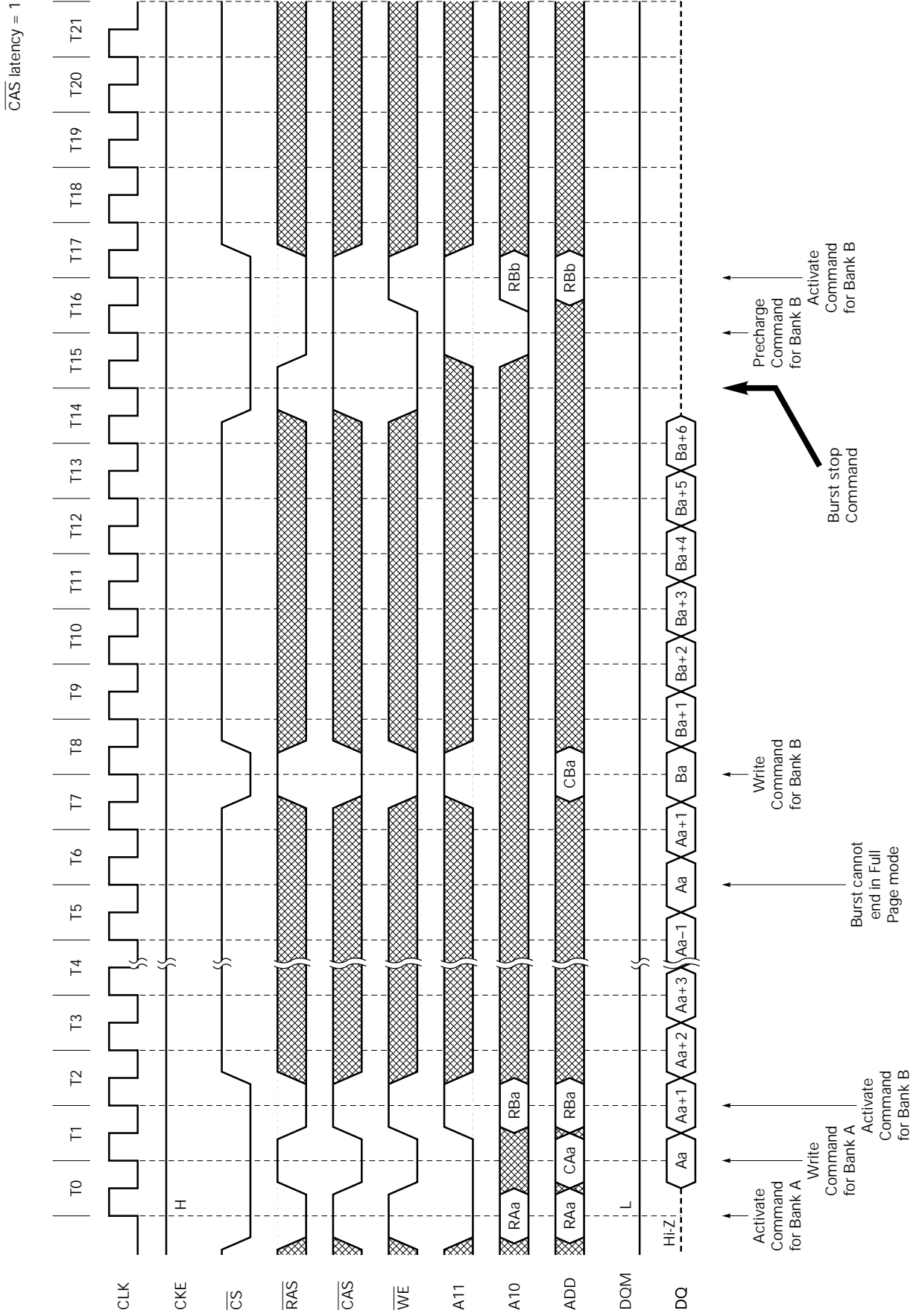


Full Page READ Cycle (3/3)

CAS latency = 3

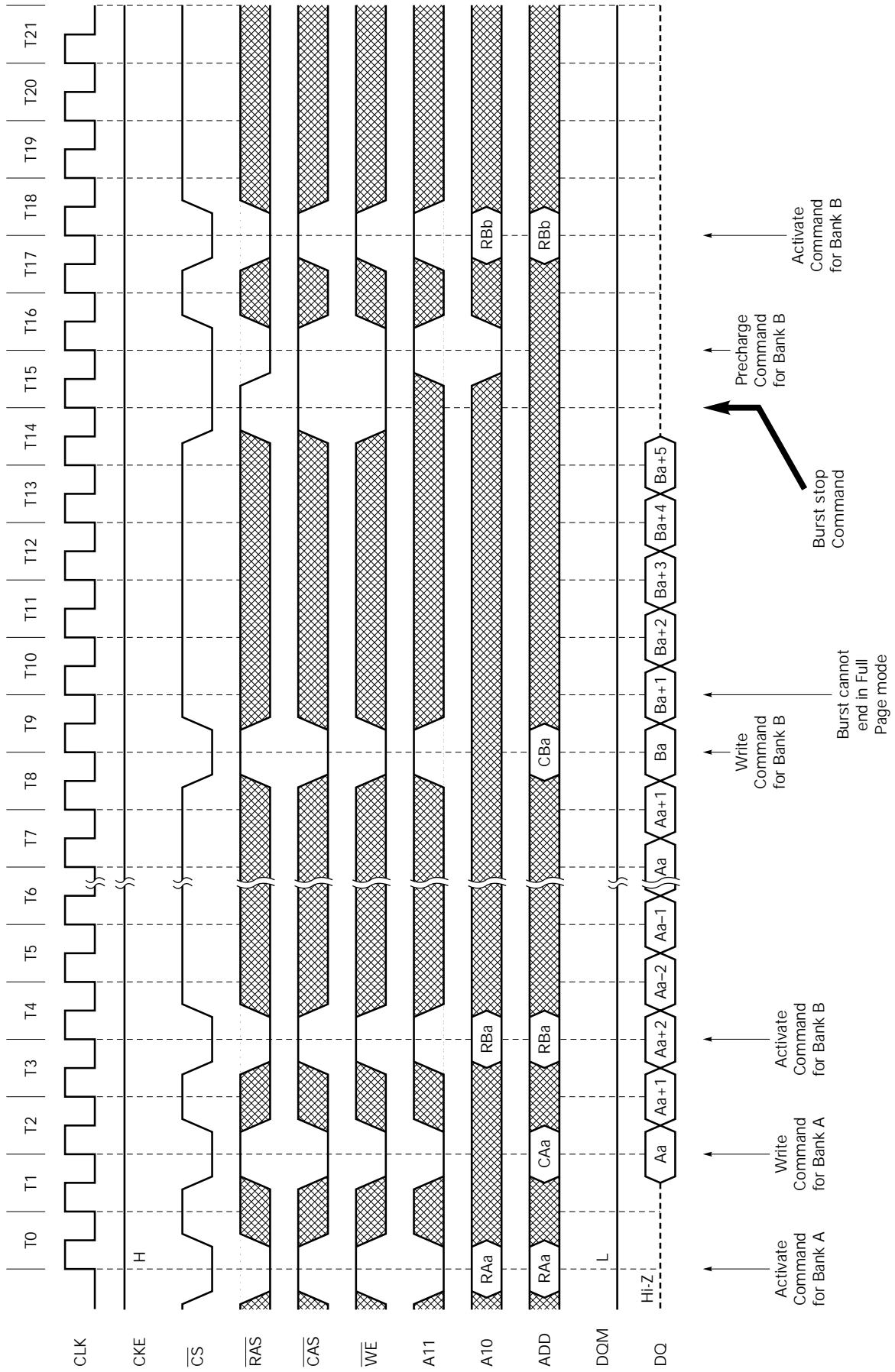


12.22 Full Page WRITE Cycle (1/3)



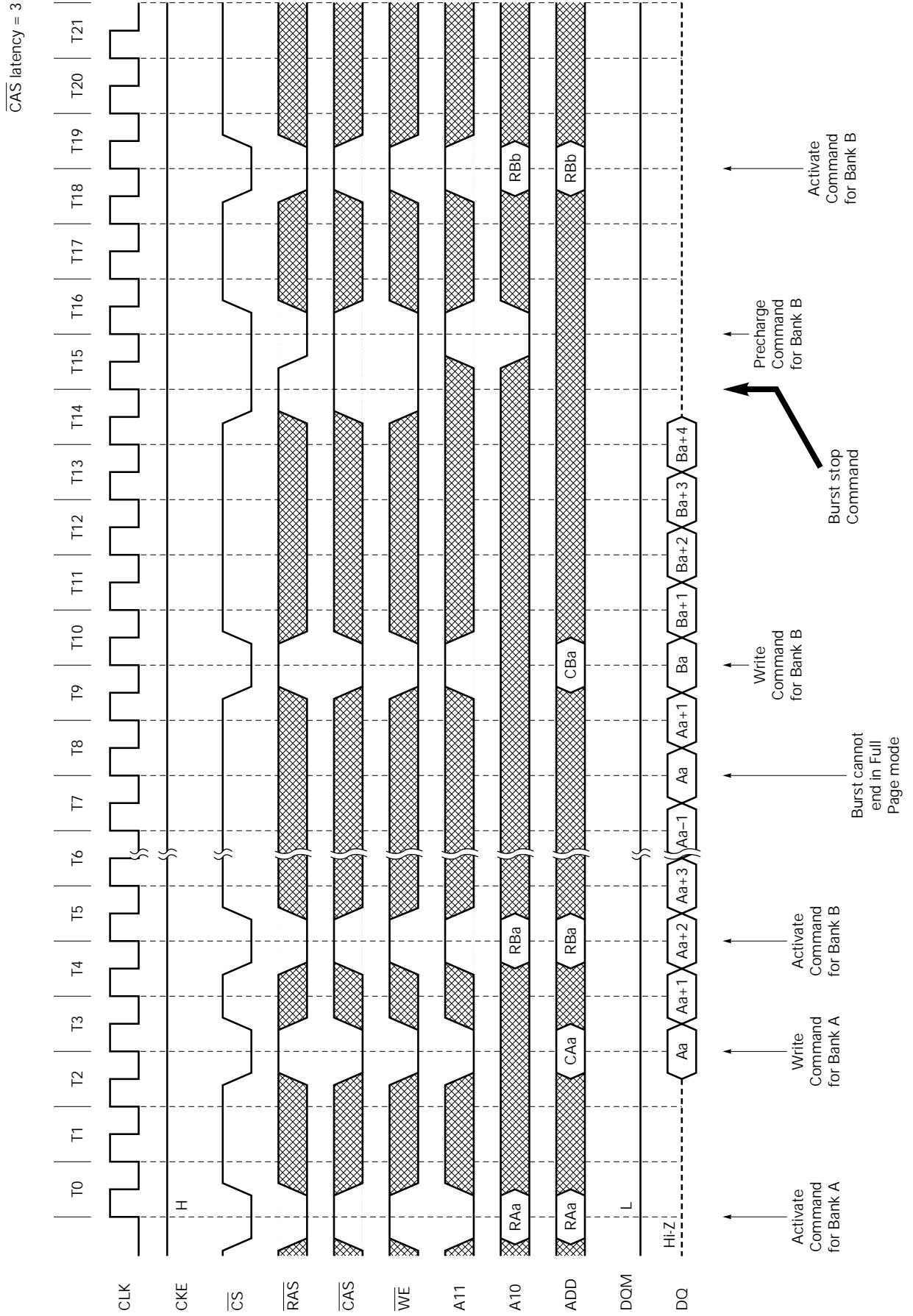
Full Page WRITE Cycle (2/3)

CAS latency = 2



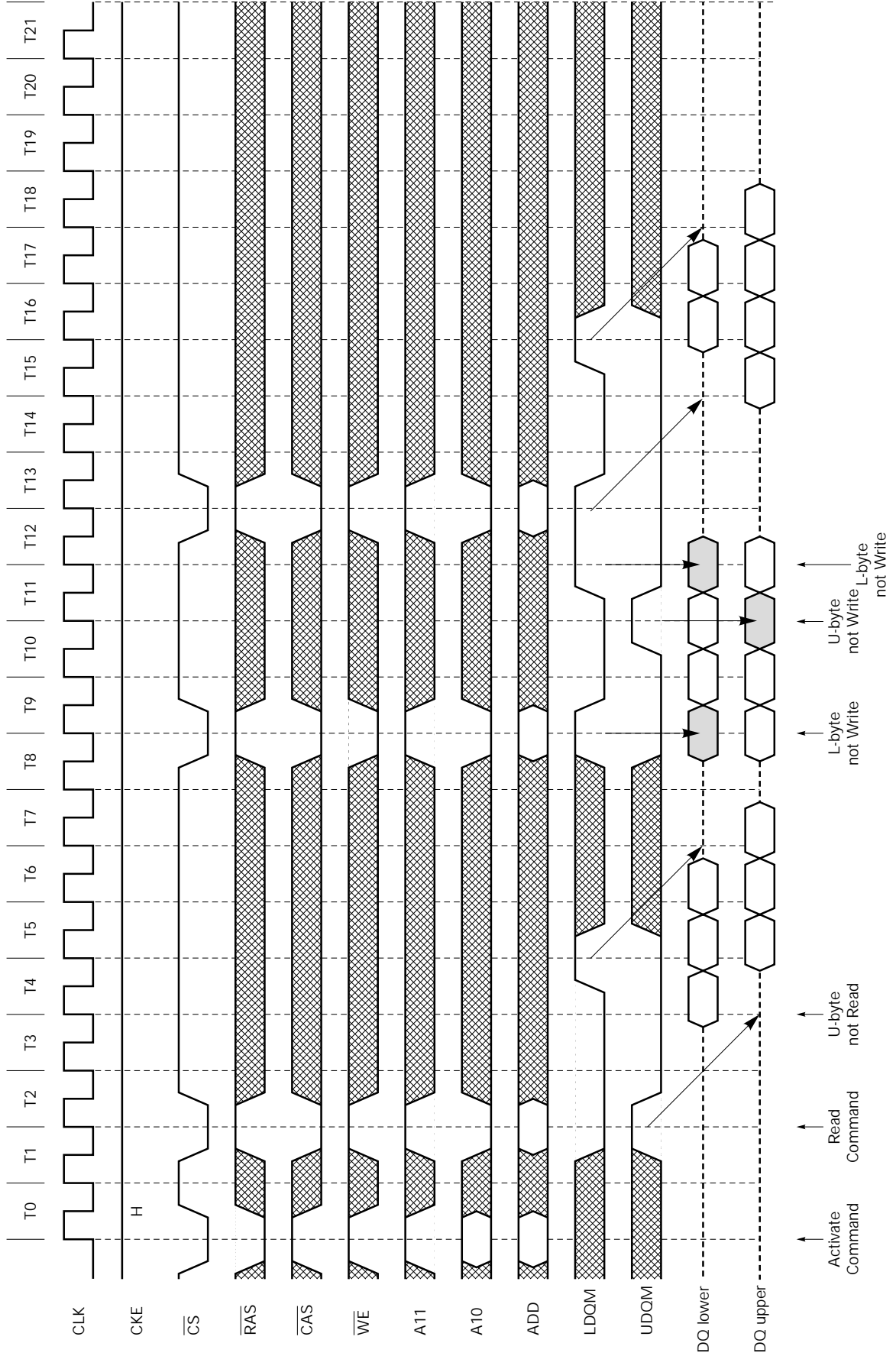


Full Page WRITE Cycle (3/3)

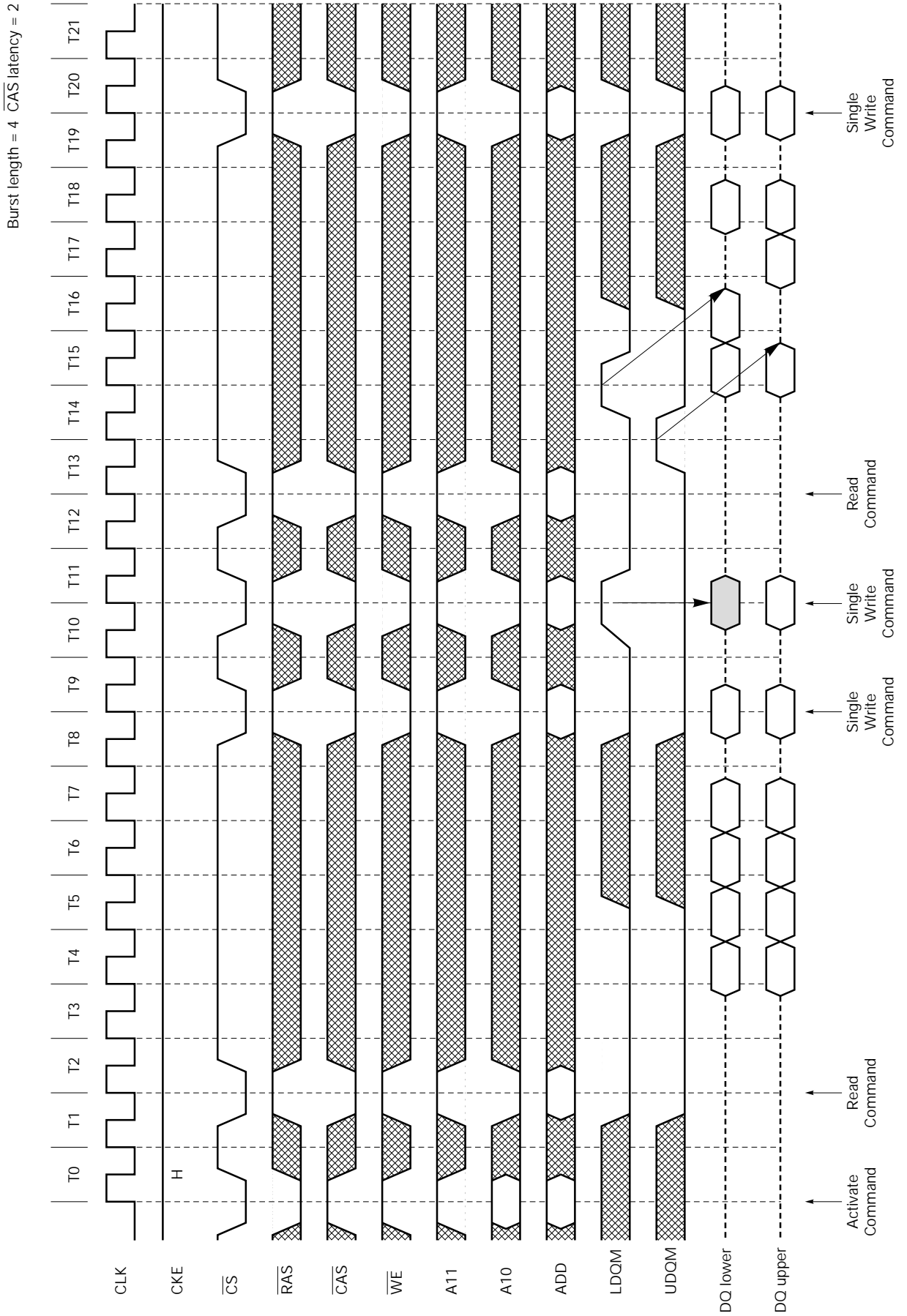


12.23 Byte Write Operation

Burst length = 4  $\overline{\text{CAS}}$  latency = 2



12.24 Burst Read and Single Write (Option)

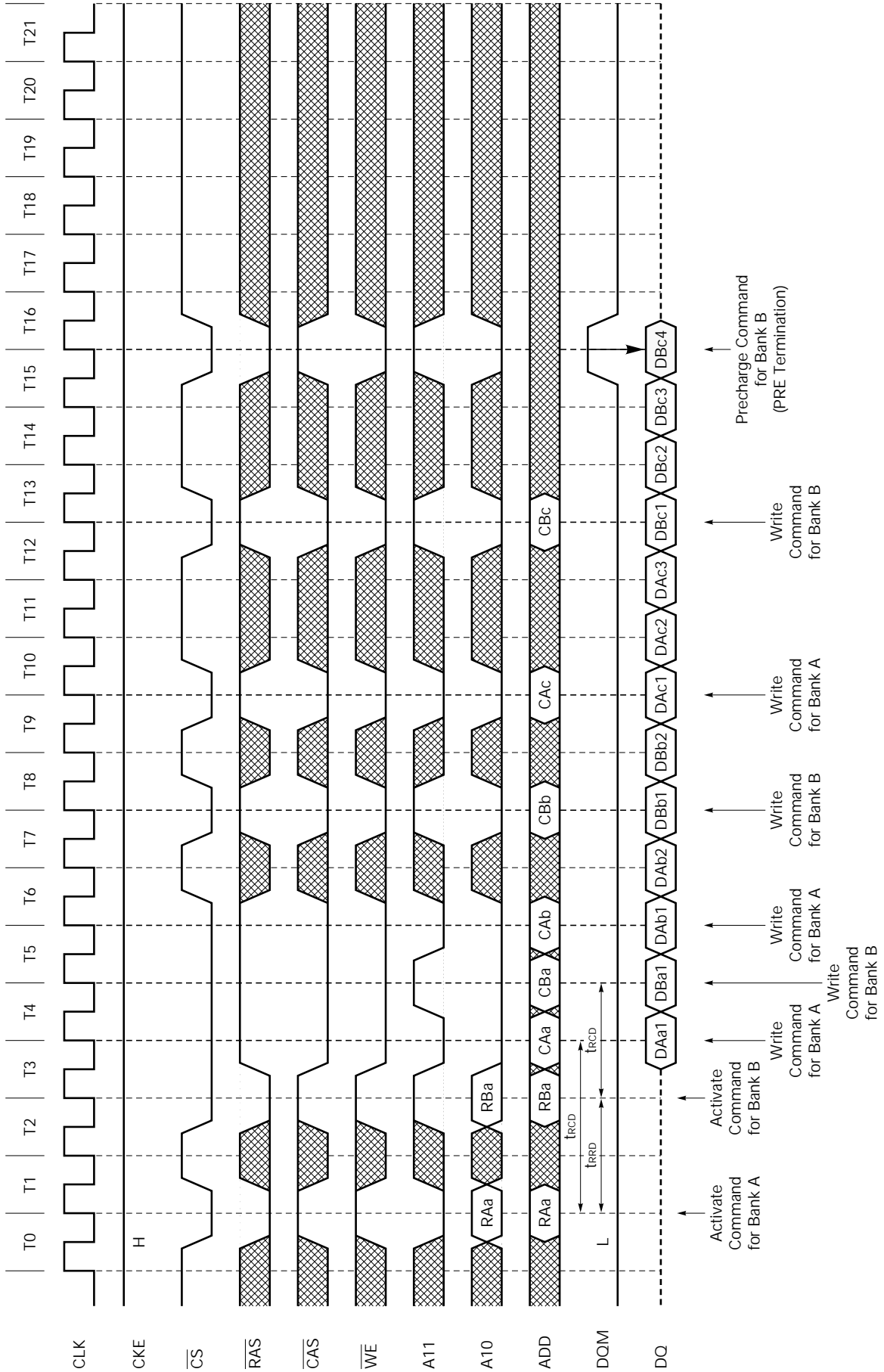




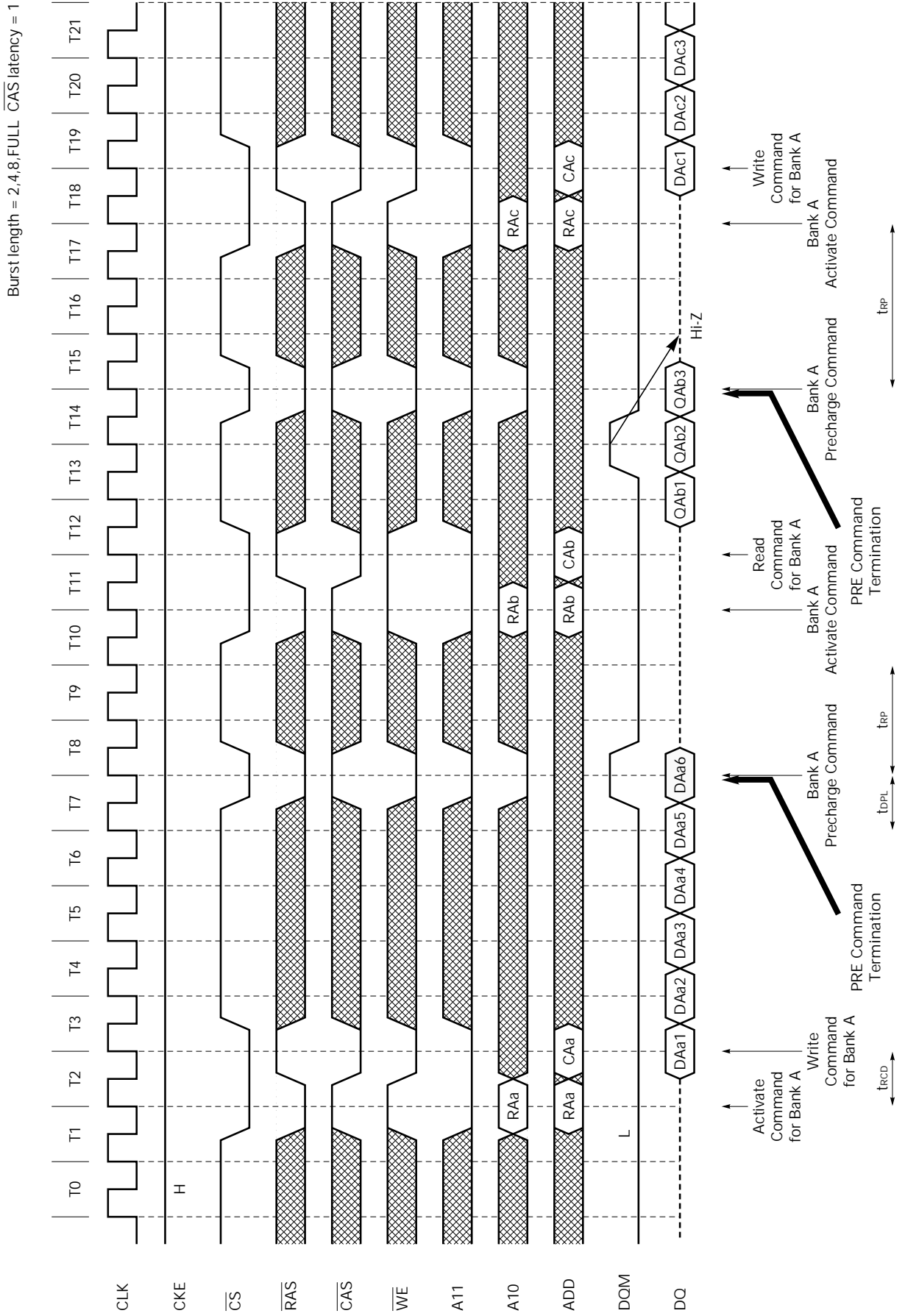


12.27 Full Page Random Column Write

Burst length = Full Page CAS latency = 2

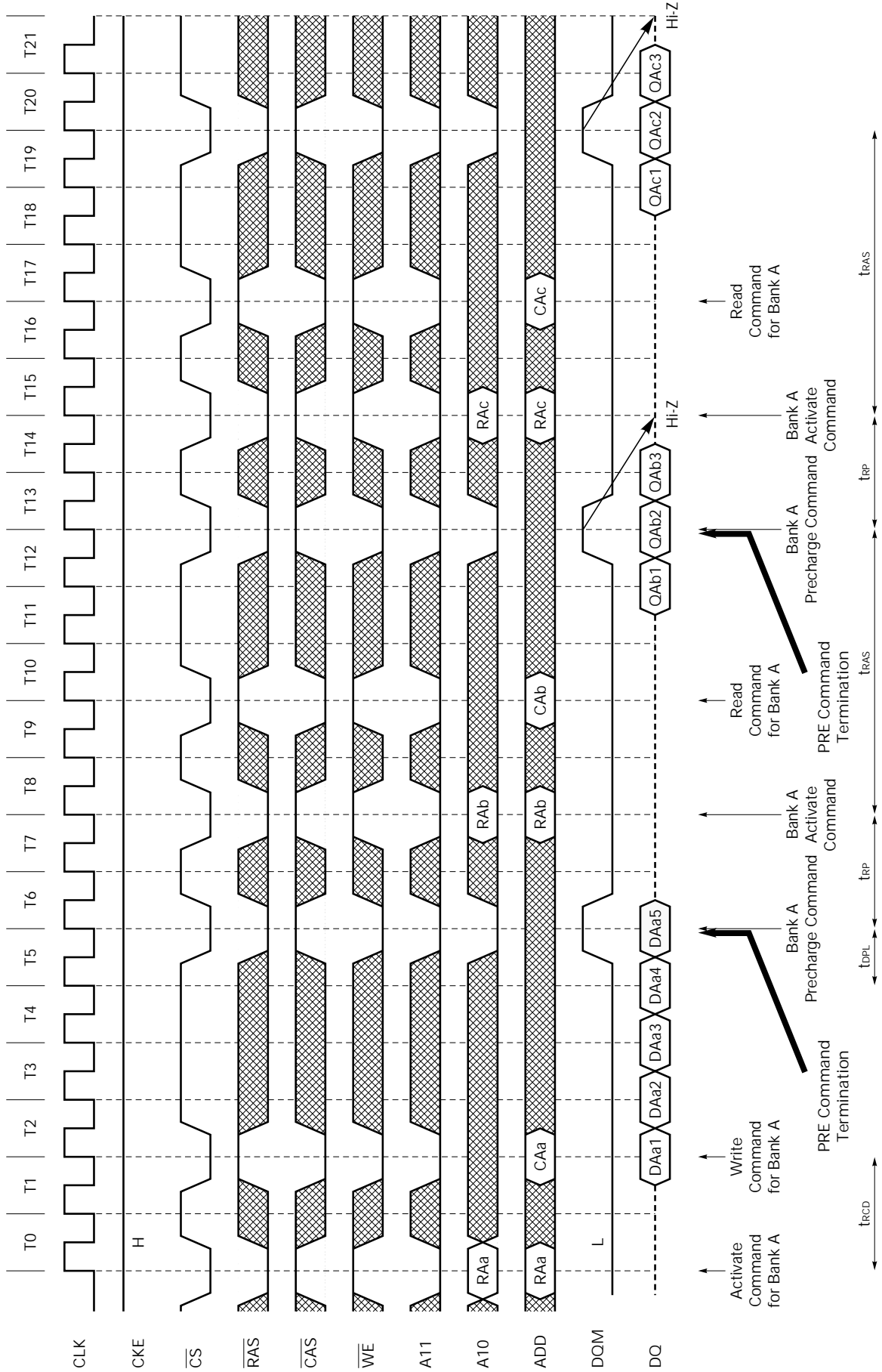


12.28 PRE(Precharge)Termination of Burst (1/3)



PRE(Precharge)Termination of Burst (2/3)

Burst length = 2,4,8,FULL, CAS latency = 2

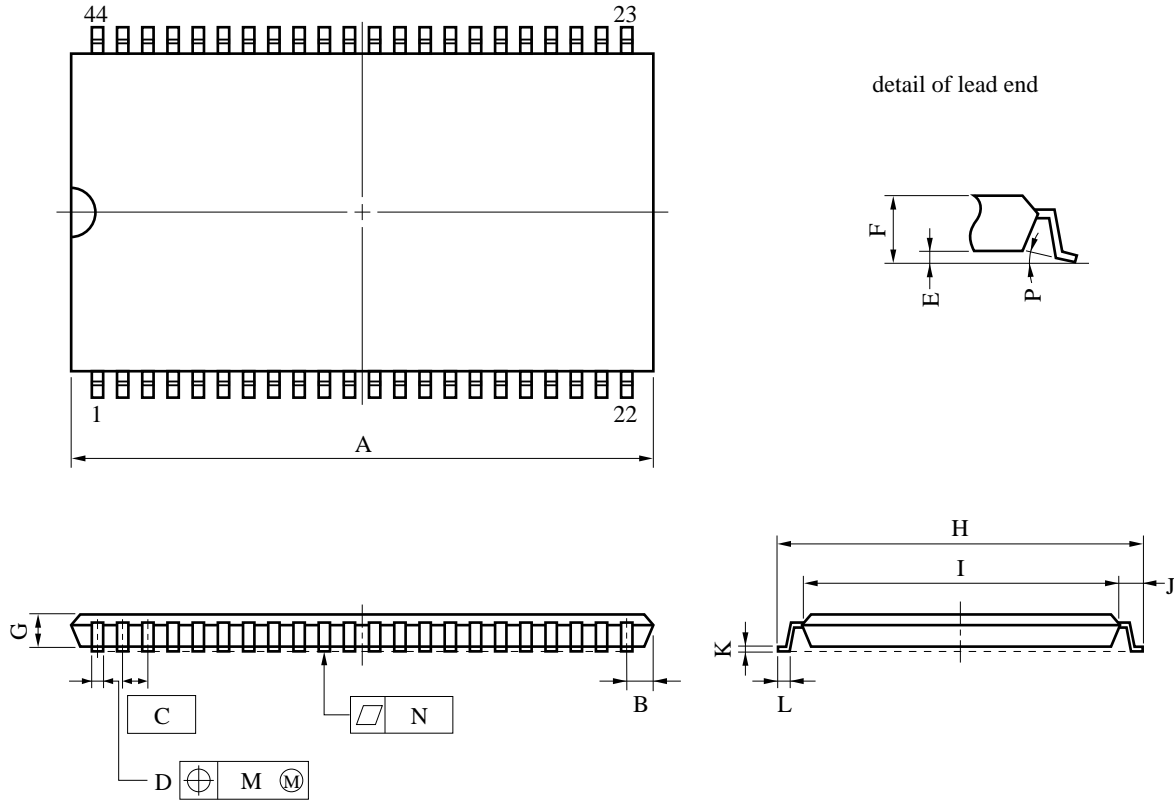






13. Package Drawings

44PIN PLASTIC TSOP(II) (400 mil)

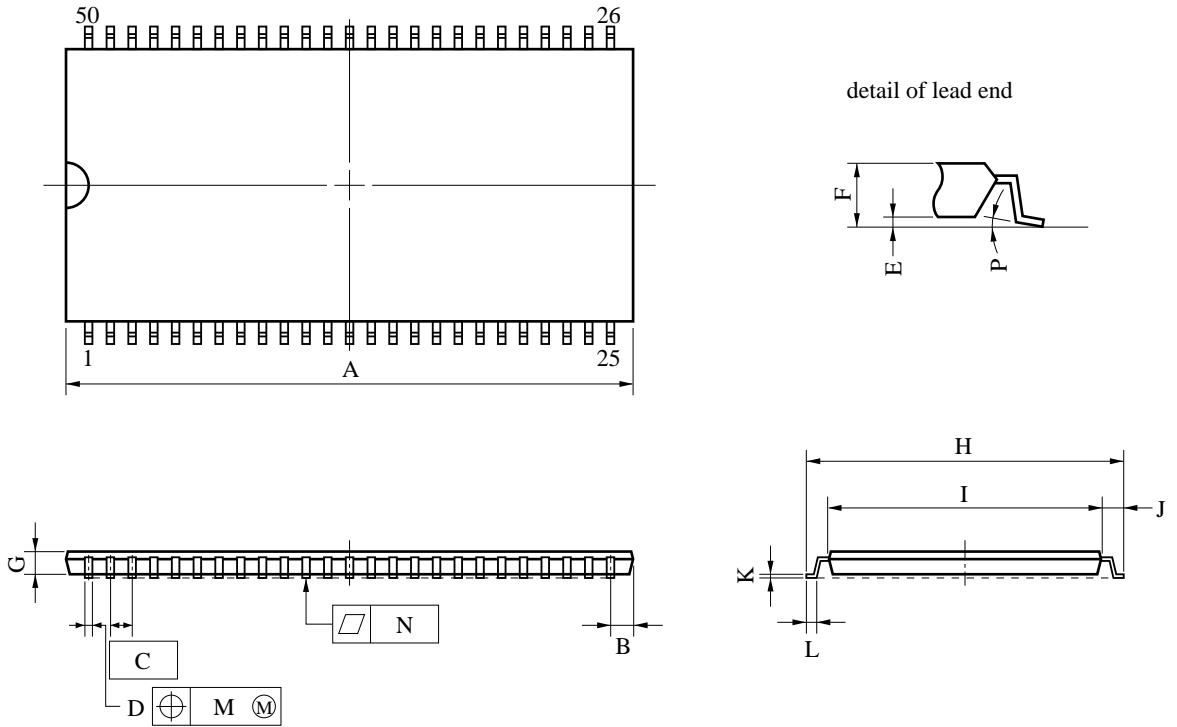


NOTE  
 Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	0.93 MAX.	0.037 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.32 <sup>+0.08</sup> / <sub>-0.07</sub>	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 <sup>+0.009</sup> / <sub>-0.008</sub>
K	0.145 <sup>+0.025</sup> / <sub>-0.015</sub>	0.006±0.001
L	0.5±0.1	0.020 <sup>+0.004</sup> / <sub>-0.005</sub>
M	0.13	0.005
N	0.10	0.004
P	3 <sup>+7</sup> / <sub>-3</sub>	3 <sup>+7</sup> / <sub>-3</sub>

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50PIN PLASTIC TSOP(II) (400 mil)



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.32 <sup>+0.08</sup> / <sub>-0.07</sub>	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 <sup>+0.009</sup> / <sub>-0.008</sub>
K	0.145 <sup>+0.025</sup> / <sub>-0.015</sub>	0.006±0.001
L	0.5±0.1	0.020 <sup>+0.004</sup> / <sub>-0.005</sub>
M	0.13	0.005
N	0.10	0.004
P	3 <sup>+7</sup> / <sub>-3</sub>	3 <sup>+7</sup> / <sub>-3</sub>

S50G5-80-7JF3

#### 14. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the  $\mu$ PD4516421, 4516821, 4516161.

#### Types of Surface Mount Device

$\mu$ PD4516421G5-7JF, 4516821G5-7JF: 44-pin Plastic TSOP (II) (400 mil)

$\mu$ PD4516161G5-7JF: 50-pin Plastic TSOP (II) (400 mil)

## NOTES FOR CMOS DEVICES

## ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

## ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

## ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.